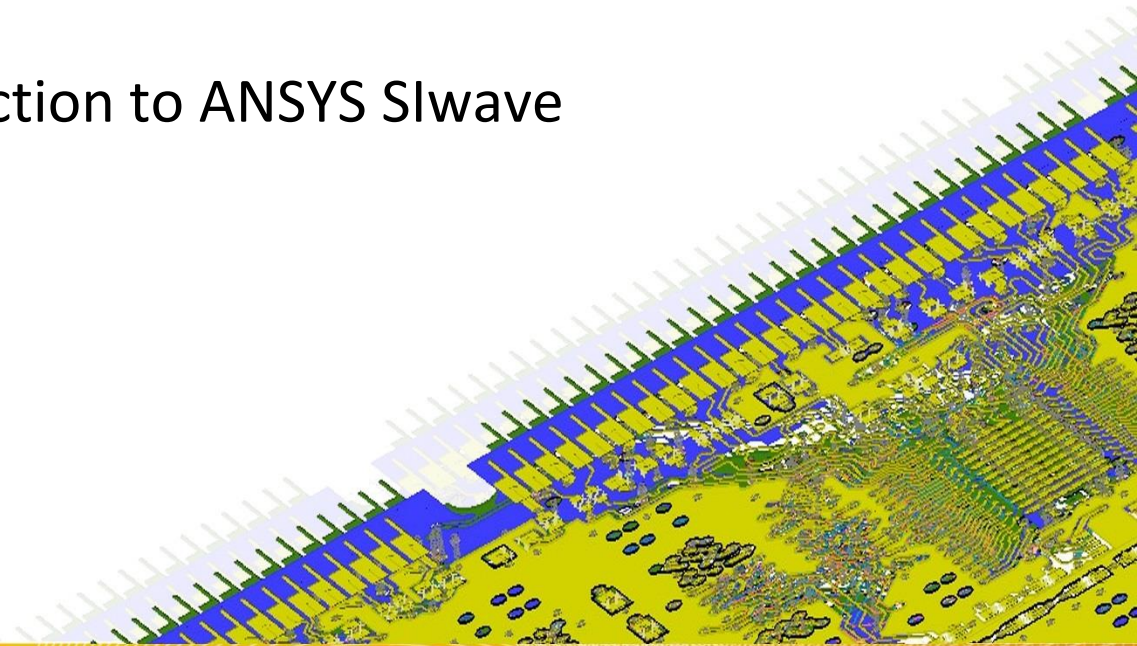




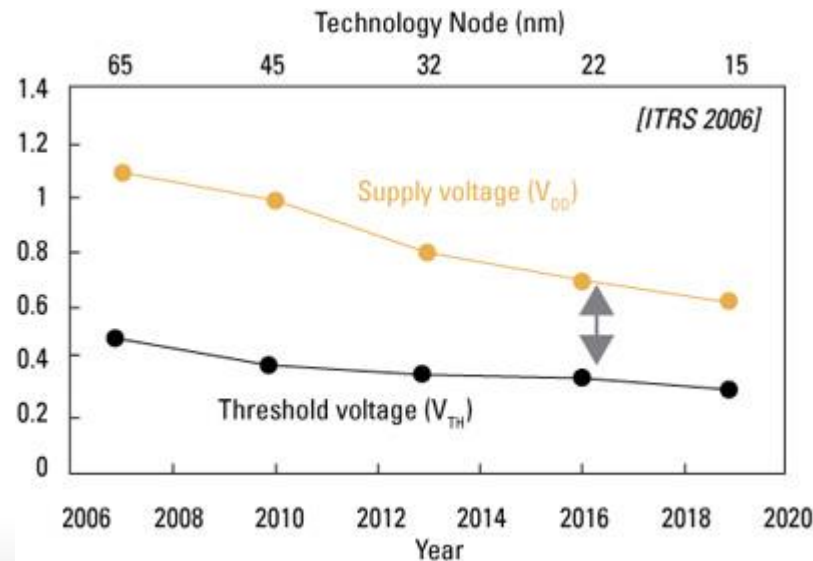
Session 1 - DC Analysis with Siwave

Introduction to ANSYS Siwave



Why is it important to run DC IR simulations?

- Supplying clean and sufficient power to today's high speed semiconductors is a major bottleneck in the industry.
- With the trend of adding more functionality into every integrated circuit, the design challenges of being able to operate many different IC functions into an ever shrinking area has proven to be one of the biggest challenges to Power Integrity engineers.
- Being able to simulate these power rails has become critical to design systems that:
 - Avoid DC current crowding in planes, traces and vias which can lead to PCB failures and bad circuit performance.
 - Debug existing PCB designs to make minor layout changes that result in major performance and reliability improvements.
 - Reduce design spins
 - Decrease warranty costs associated with thermal-cycling issues.



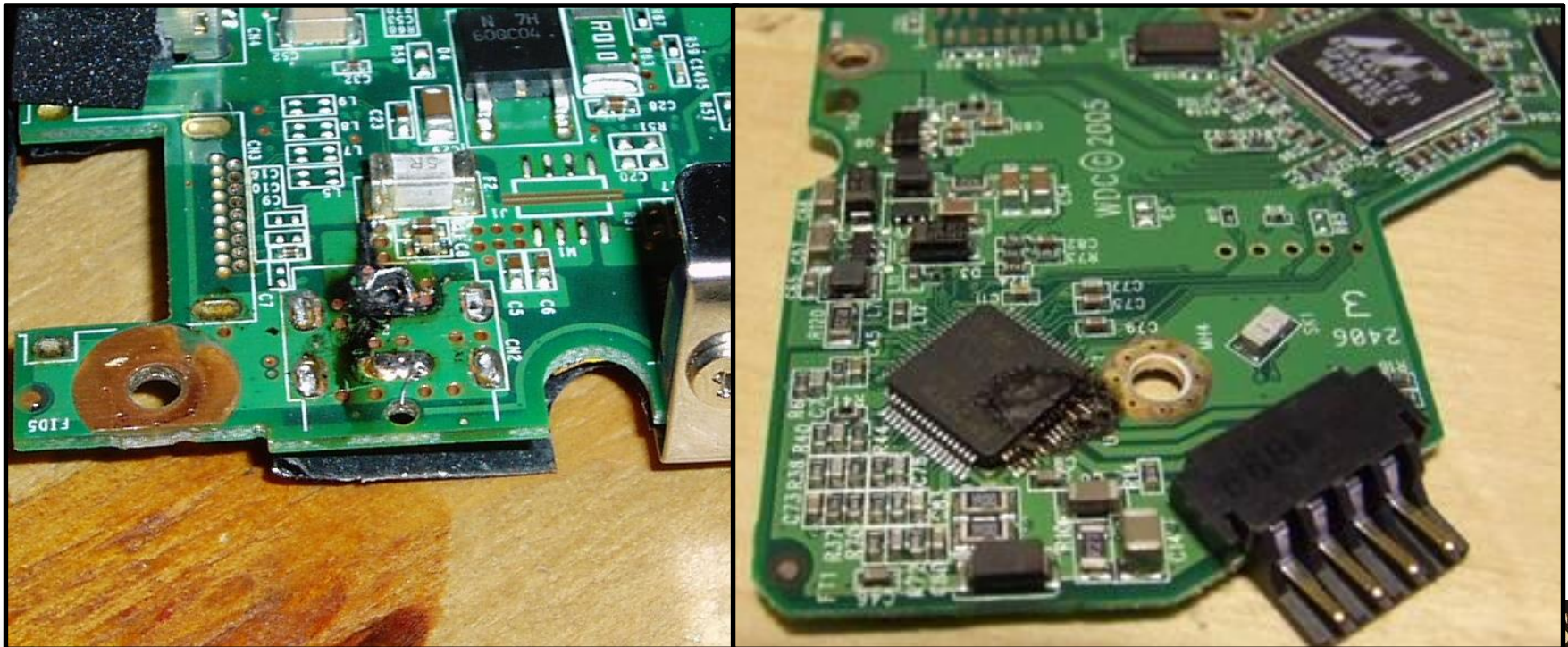
The Importance of DC Simulations

Failures

- Lack of good DC design may not lead to high DC resistance but it can cause “thermal hot spots” due to excessive temperatures and eventual product failure.

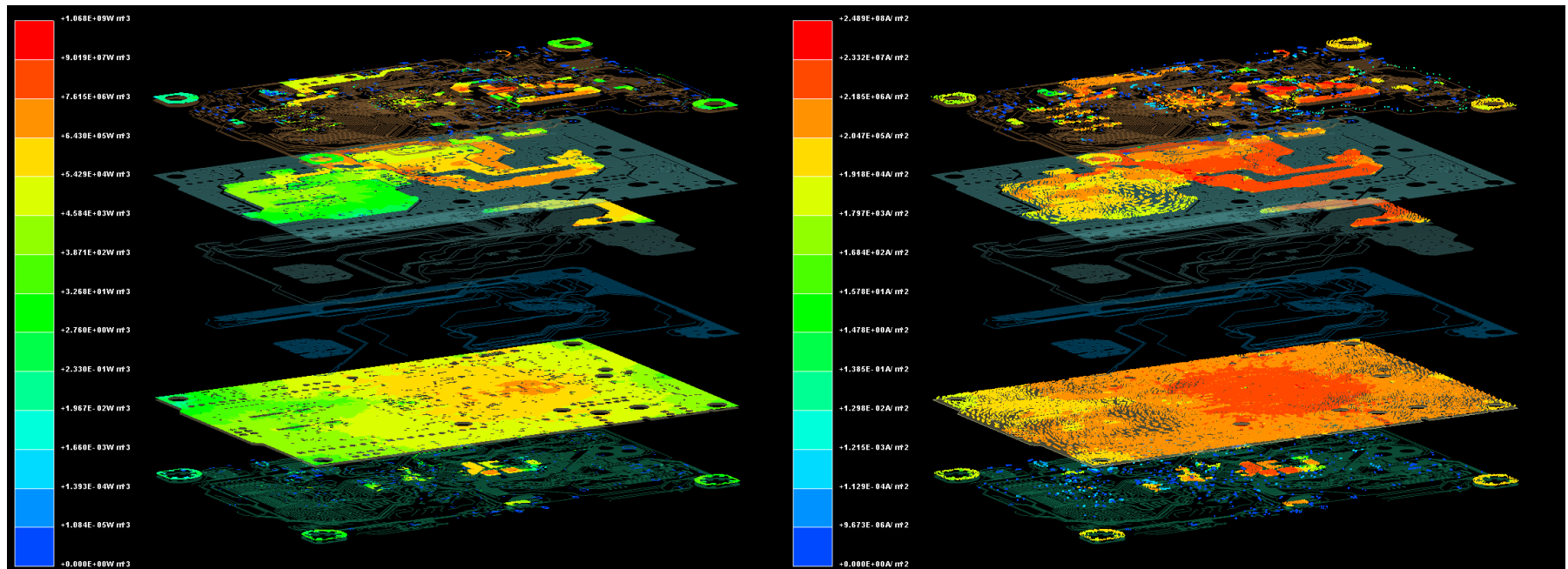
Solution

- Robust and accurate DC and PDN design results in a more even spread of current density and reduces risk of failure.

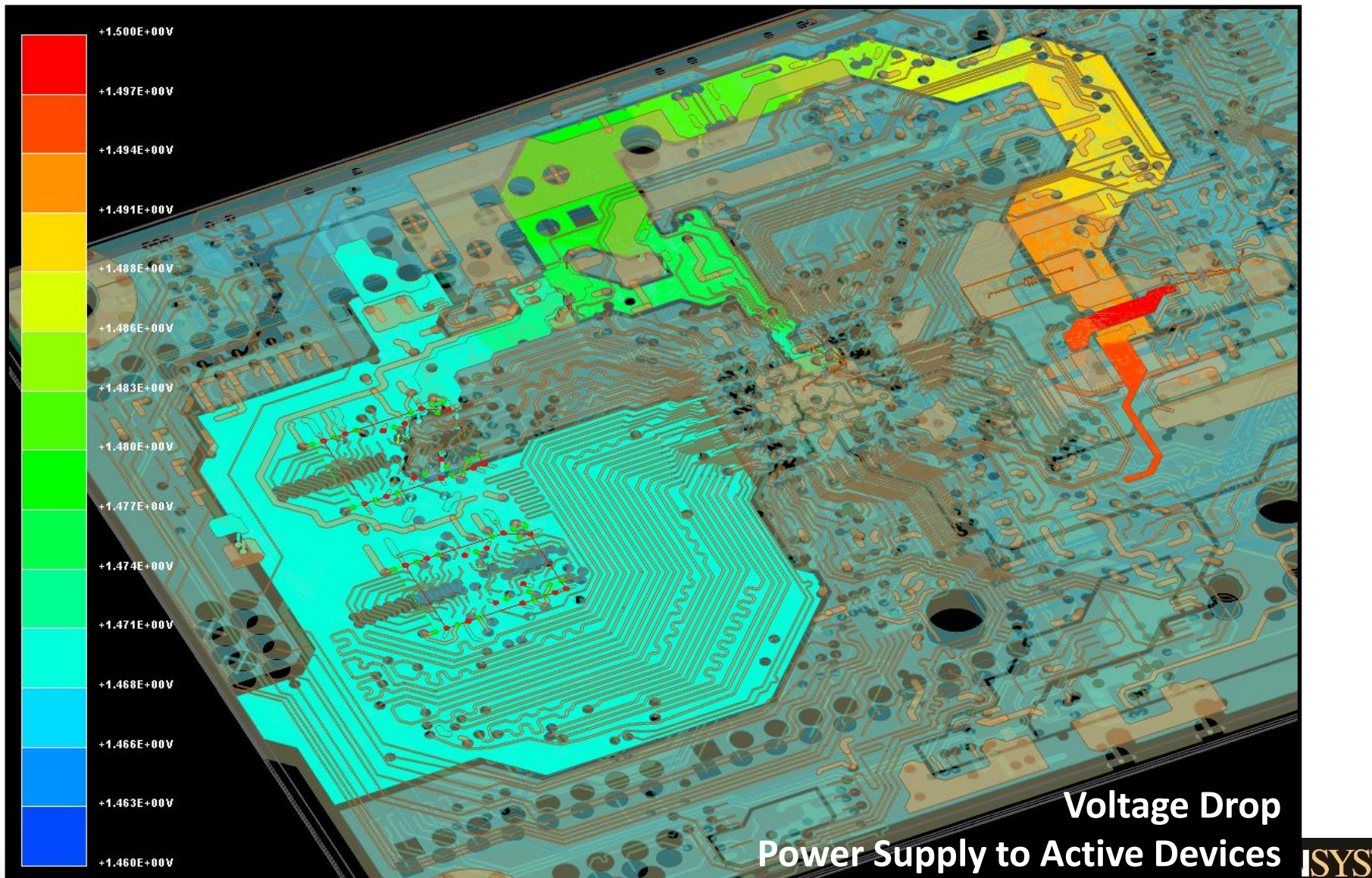


Siwave R16 Solutions

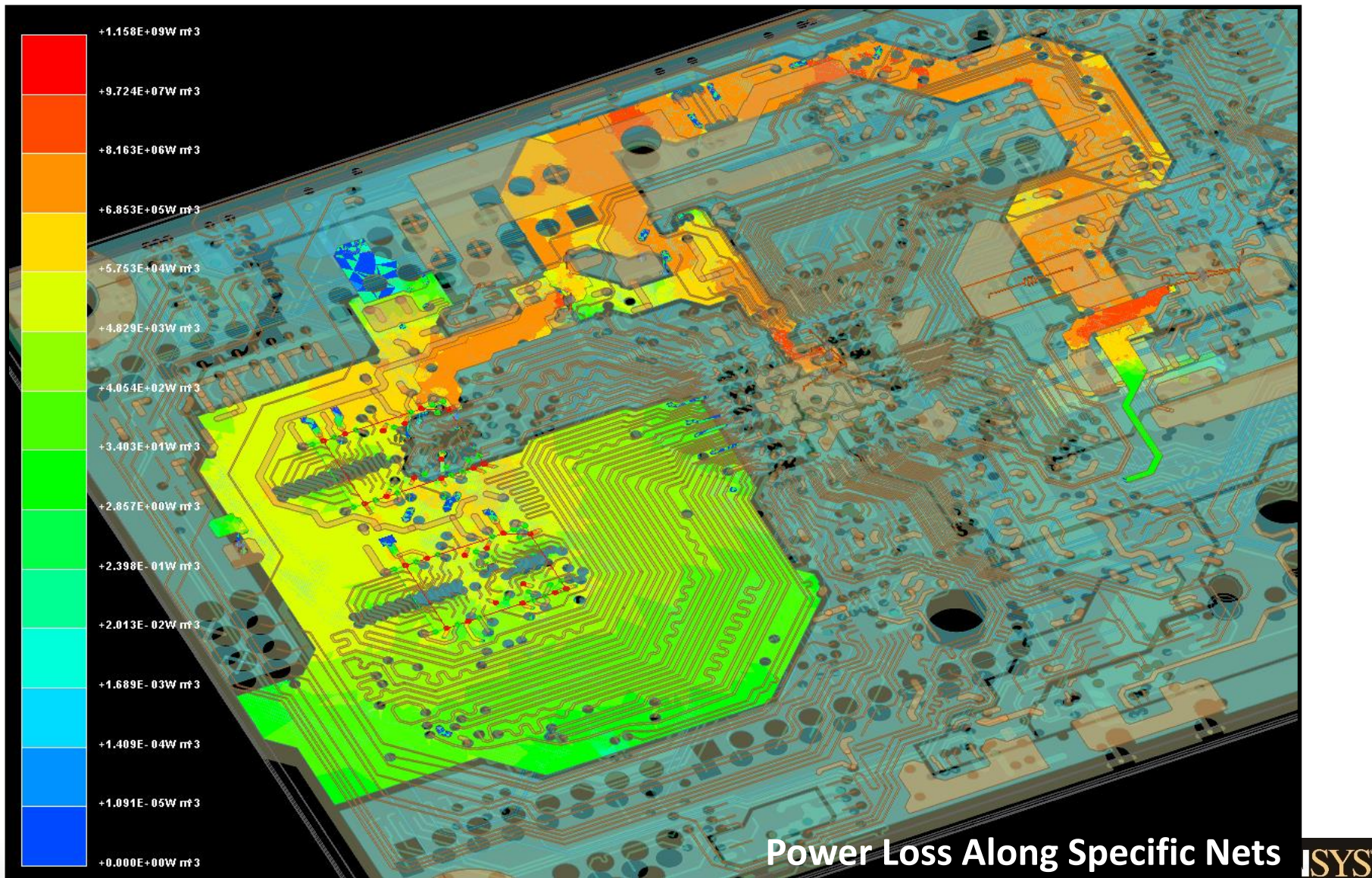
- **Siwave-DC** – Includes all the essentials to import, setup, and view results for DC simulations. It can handle large geometries and even combine Chip, Package and Board together. Results include:
 - DC IR drop (Voltage) for all nets including Power, Ground, and Signals.
 - DC current distribution (Amperes/Area²) including return paths.
 - DC current magnitude (Amperes) into and out of vias.
 - Power density (W/Area²) and total power loss (Watts) per layer.
 - Automated report generation with user defined pass/fail criteria.
 - Bi-directional coupling to Icepak for thermal loss simulations (joule heating).



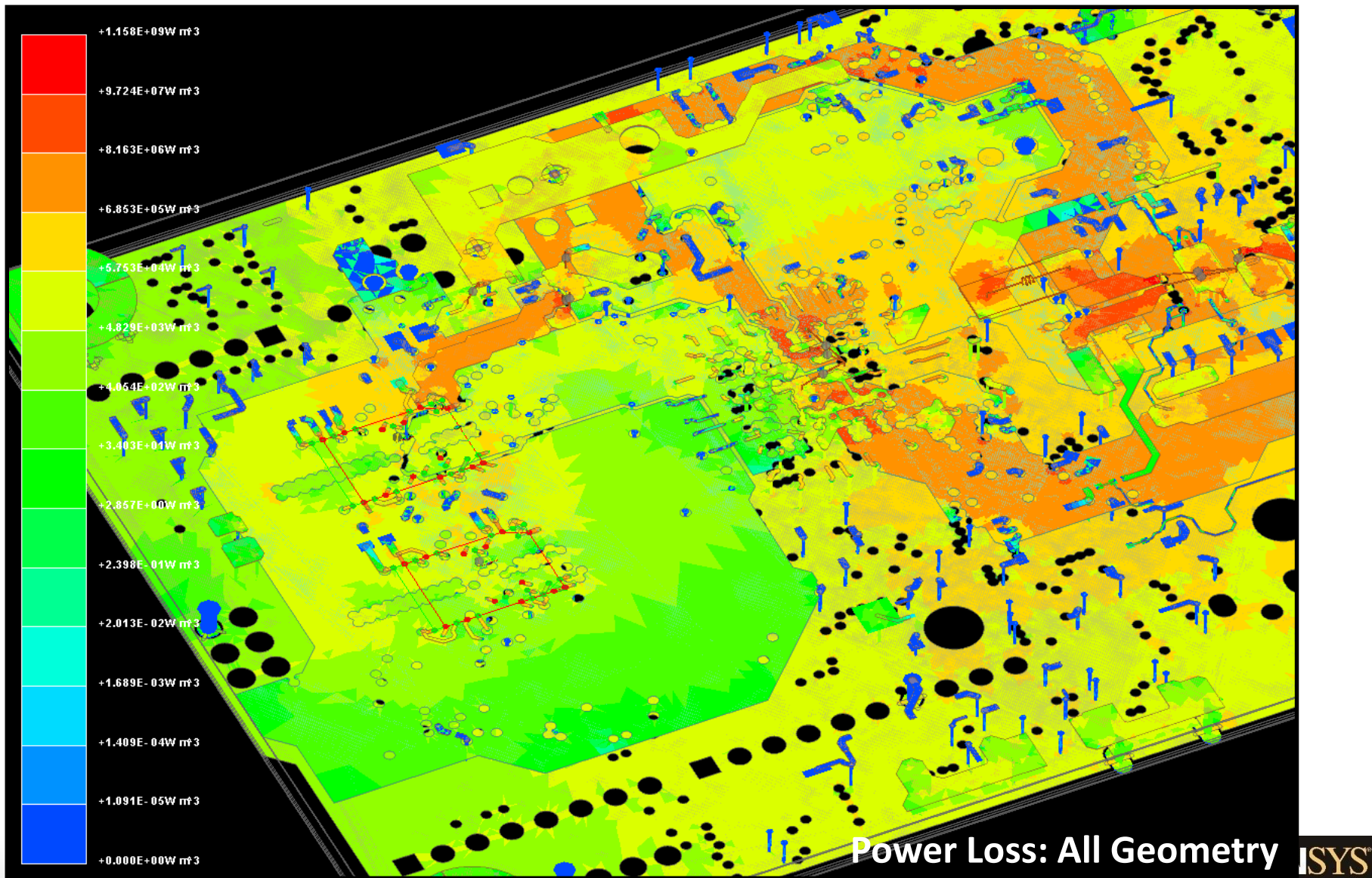
Overview: IR Drop with SIwave-DC



Overview: IR Drop with SIwave-DC



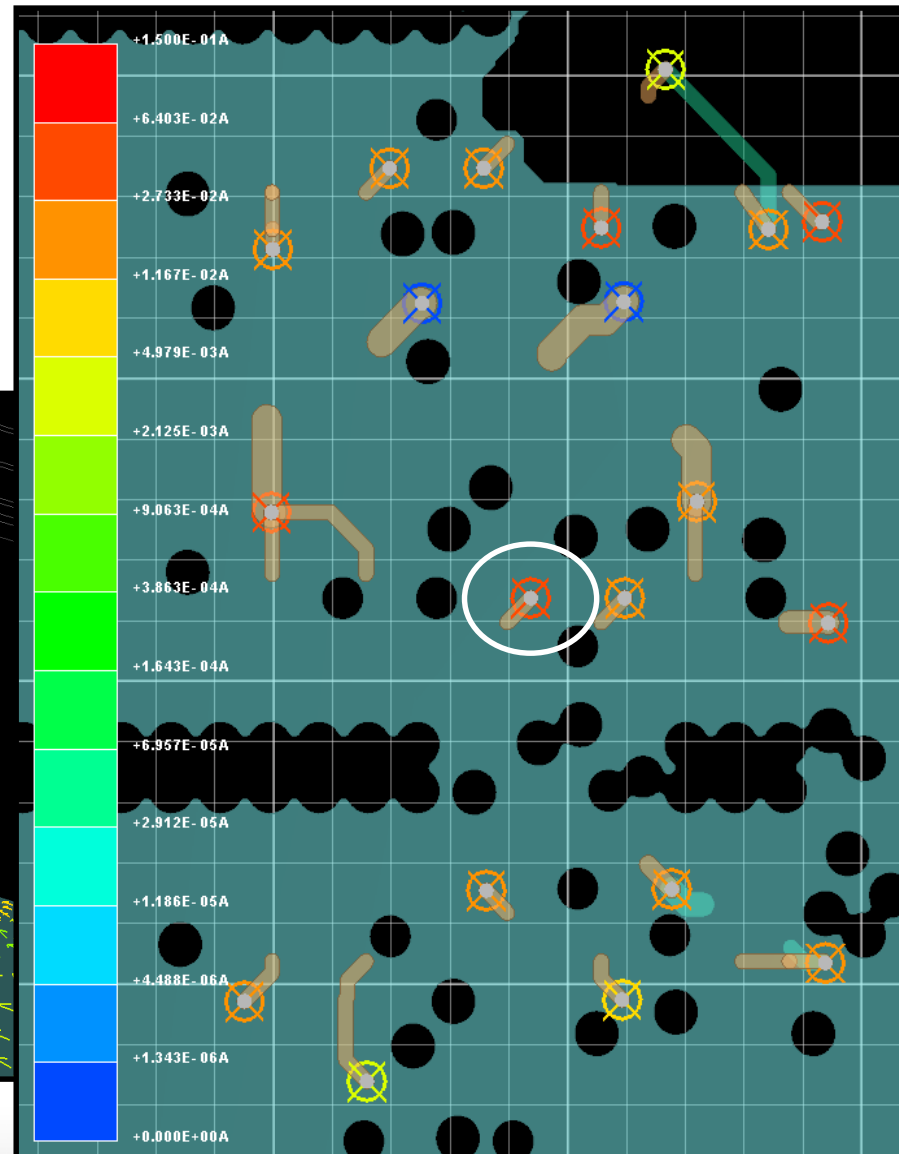
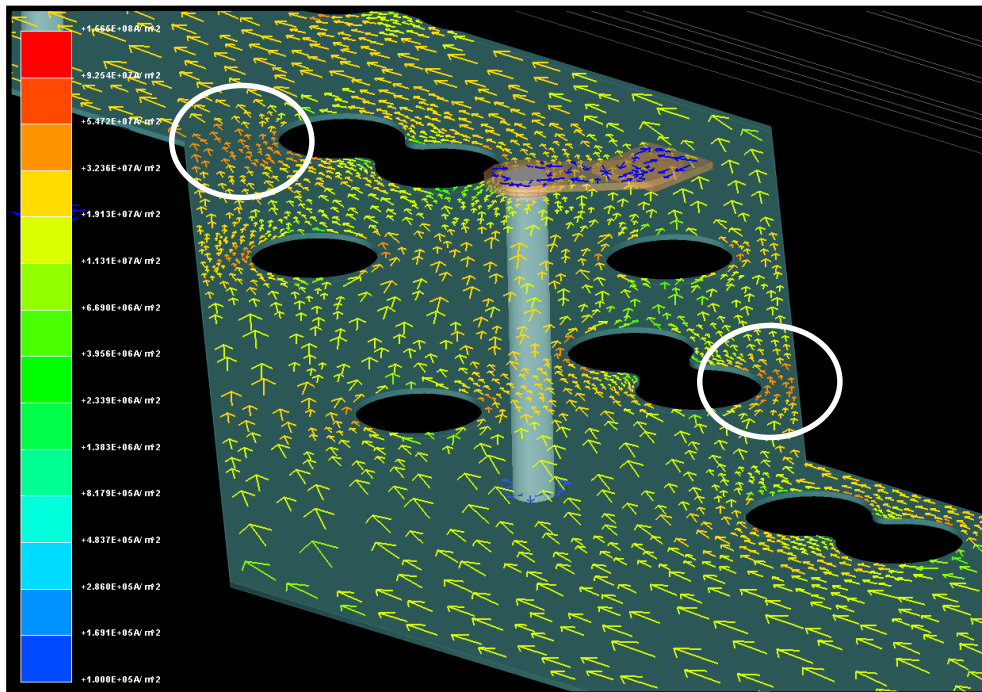
Overview: IR Drop with SIwave-DC



Overview: IR Drop with SIwave-DC

Quickly Identify:

- High Currents in Vias
- Current Crowding in Copper
- High Power Loss Regions



Overview: SIwave-DC Tabular Element Data

DC Simulation Element Data(DC_2)

Bondwires Current Sources Metallization Vias Voltage Probes Voltage Sources

| Via | Net | x (mm) | y (mm) | Current / A | Limit / A | Pass / Fail | Resistance / Ohms | IR Drop / V | Power / W |
|--------------------|-------------|------------|------------|----------------------|--------------------|-------------|--------------------|---------------------|--------------------|
| Via 41 (TOP-PWR) | V1P5_S5 | 4.3815e+01 | 3.8430e+01 | -1.000000000268e+00 | 4.560367311877e+00 | Pass | 3.679195470795e-04 | -3.679195471780e-04 | 3.679195472766e-04 |
| Via 17 (TOP-PWR) | V3P3_S5 | 5.6718e+01 | 4.0183e+01 | 9.077472854881e-01 | 4.560367311877e+00 | Pass | 3.679195470712e-04 | 3.339779701319e-04 | 3.031675958001e-04 |
| Via 14 (TOP-PWR) | V3P3_S5 | 4.3197e+01 | 4.0430e+01 | -8.487438187733e-01 | 4.560367311877e+00 | Pass | 3.679195471095e-04 | -3.122694414150e-04 | 2.650367581928e-04 |
| Via 13 (TOP-PWR) | V3P3_S5 | 4.3197e+01 | 3.9719e+01 | -7.012561819695e-01 | 4.560367311877e+00 | Pass | 3.679195470617e-04 | -2.580058568444e-04 | 1.809282020965e-04 |
| Via 336 (TOP-GND) | GND | 7.2847e+01 | 3.0785e+01 | -6.746616582421e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -9.584826284337e-04 | 6.466514794953e-04 |
| Via 337 (TOP-GND) | GND | 7.3838e+01 | 3.3858e+01 | -6.442200334569e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -9.152346267407e-04 | 5.896124818598e-04 |
| Via 326 (TOP-GND) | GND | 7.0256e+01 | 3.6678e+01 | -6.351798386271e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -9.023913450806e-04 | 5.731807889468e-04 |
| Via 331 (TOP-GND) | GND | 7.0155e+01 | 3.4315e+01 | -6.288235601626e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -8.933610668437e-04 | 5.617664865633e-04 |
| Via 116 (TOP-P... | V1P0_S0 | 4.2189e+01 | 3.4366e+01 | -6.225530471388e-01 | 4.560367311877e+00 | Pass | 3.679195470702e-04 | -2.290494351305e-04 | 1.425954237859e-04 |
| Via 16 (TOP-PWR) | V3P3_S5 | 5.7480e+01 | 4.0157e+01 | 5.870835283683e-01 | 4.560367311877e+00 | Pass | 3.679195470715e-04 | 2.159995058504e-04 | 1.268097520205e-04 |
| Via 339 (TOP-GND) | GND | 7.4371e+01 | 3.1471e+01 | -5.826294964863e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -8.277337897789e-04 | 4.822621211636e-04 |
| Via 338 (TOP-GND) | GND | 7.4371e+01 | 3.2283e+01 | -5.781934063896e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -8.214314970016e-04 | 4.749462753671e-04 |
| Via 15 (TOP-PWR) | V3P3_S5 | 5.7455e+01 | 4.0869e+01 | 5.410141362950e-01 | 4.560367311877e+00 | Pass | 3.679195470707e-04 | 1.990496759845e-04 | 1.076886885326e-04 |
| Via 114 (TOP-P... | V1P0_S0 | 4.1377e+01 | 3.3553e+01 | -5.293055399897e-01 | 4.560367311877e+00 | Pass | 3.679195470701e-04 | -1.947418545347e-04 | 1.030779424731e-04 |
| Via 7 (TOP-LYR_1) | V3P3_S5 | 7.8740e+01 | 5.9868e+01 | -5.0000000006871e-01 | 4.560367311877e+00 | Pass | 7.185537351264e-04 | -3.592768680569e-04 | 1.796384324753e-04 |
| Via 330 (TOP-GND) | GND | 6.9215e+01 | 3.4341e+01 | -4.980358800700e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -7.075527911689e-04 | 3.523866770458e-04 |
| Via 19 (TOP-PWR) | V3P3_S5 | 5.8242e+01 | 4.0132e+01 | 4.686635285079e-01 | 4.560367311877e+00 | Pass | 3.679195470698e-04 | 1.724304731368e-04 | 8.081187396258e-05 |
| Via 118 (TOP-P... | V1P0_S0 | 4.2189e+01 | 3.5179e+01 | -4.660270635844e-01 | 4.560367311877e+00 | Pass | 3.679195470672e-04 | -1.714604661550e-04 | 7.990521756303e-05 |
| Via 327 (TOP-GND) | GND | 7.1018e+01 | 3.5611e+01 | -4.627706004377e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -6.574518887365e-04 | 3.042494053095e-04 |
| Via 333 (TOP-GND) | GND | 6.9215e+01 | 3.3401e+01 | -4.617722094834e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -6.560334883066e-04 | 3.029380333904e-04 |
| Via 124 (TOP-BO... | BST_V1P5_S5 | 5.9715e+01 | 3.2309e+01 | 4.616749848783e-01 | 4.560367311877e+00 | Pass | 1.777370442915e-03 | 8.205674723560e-04 | 3.788354753916e-04 |
| Via 335 (TOP-GND) | GND | 7.0155e+01 | 3.2461e+01 | -4.542998742148e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -6.454176433698e-04 | 2.932131541989e-04 |
| Via 123 (TOP-BO... | BST_V1P5_S5 | 5.9055e+01 | 3.2309e+01 | 4.521700627474e-01 | 4.560367311877e+00 | Pass | 1.777370442915e-03 | 8.036737046984e-04 | 3.633971894819e-04 |
| Via 125 (TOP-BO... | BST_V1P5_S5 | 5.9080e+01 | 3.1674e+01 | 4.478280750474e-01 | 4.560367311877e+00 | Pass | 1.777370442915e-03 | 7.959563840967e-04 | 3.564516153117e-04 |
| Via 18 (TOP-PWR) | V3P3_S5 | 5.8318e+01 | 4.0894e+01 | 4.460604516239e-01 | 4.560367311877e+00 | Pass | 3.679195470727e-04 | 1.641143593285e-04 | 7.320492524004e-05 |
| Via 126 (TOP-BO... | BST_V1P5_S5 | 5.9741e+01 | 3.1674e+01 | 4.389405854271e-01 | 4.560367311877e+00 | Pass | 1.777370442914e-03 | 7.801600227335e-04 | 3.424438971055e-04 |
| Via 329 (TOP-GND) | GND | 7.1018e+01 | 3.4747e+01 | -4.371168596308e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -6.210059685967e-04 | 2.714521788050e-04 |
| Via 334 (TOP-GND) | GND | 7.0155e+01 | 3.3401e+01 | -4.159429431954e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -5.909244739226e-04 | 2.457908648896e-04 |
| Via 35 (PWR-BO... | V1P5_S5 | 6.3068e+01 | 3.1750e+01 | -4.088436625751e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -5.808386226431e-04 | 2.374721898465e-04 |
| Via 445 (TOP-GND) | GND | 3.2461e+01 | 5.3442e+01 | 4.000000002947e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | 5.682745520991e-04 | 2.273098210071e-04 |
| Via 332 (TOP-GND) | GND | 7.1044e+01 | 3.3807e+01 | -3.972099637984e-01 | 4.560367311877e+00 | Pass | 1.420686379201e-03 | -5.643107852513e-04 | 2.241498665807e-04 |

Fit Selection

Export

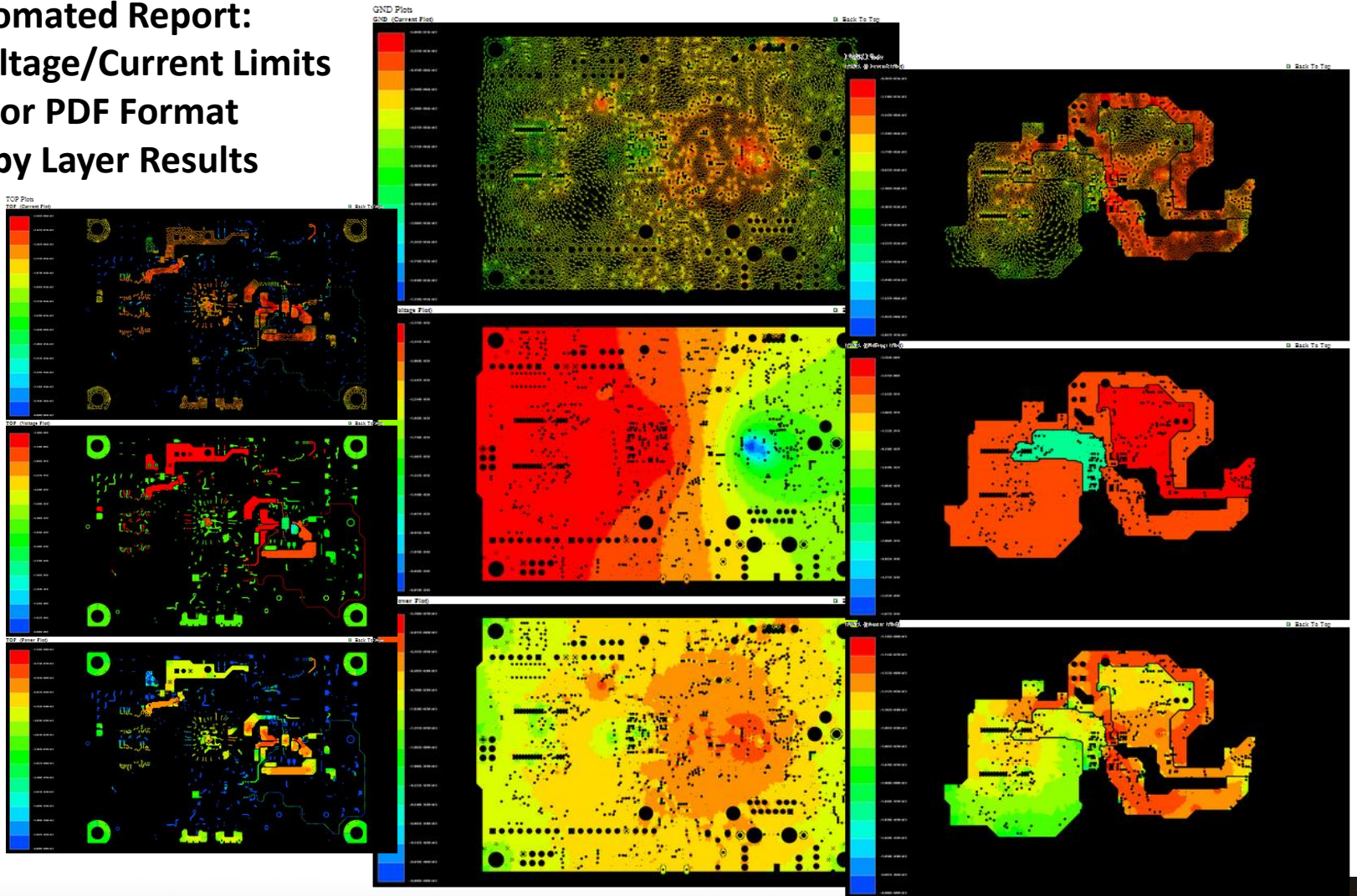
Close

All Element Data Available

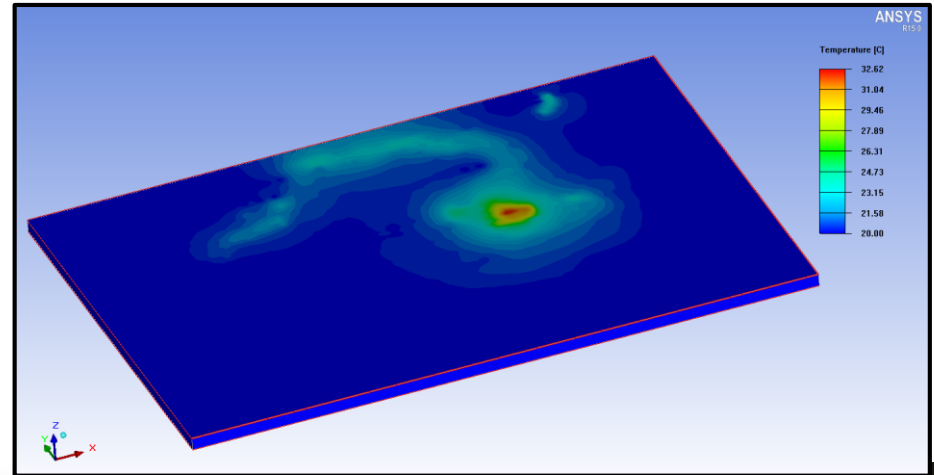
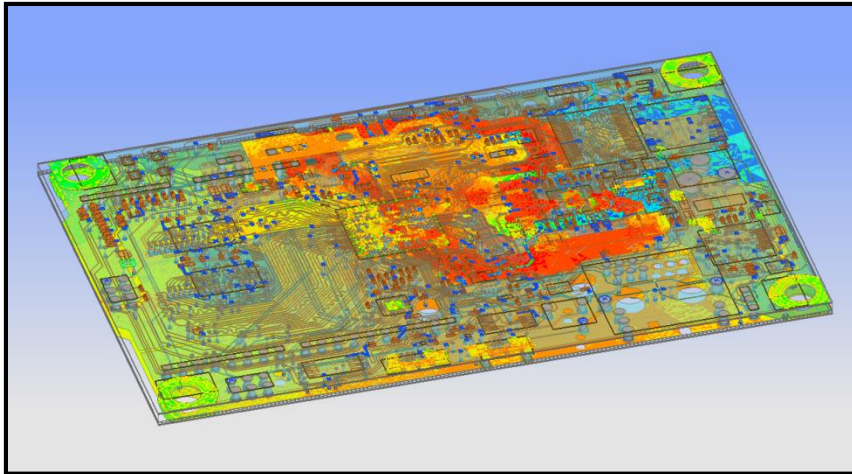
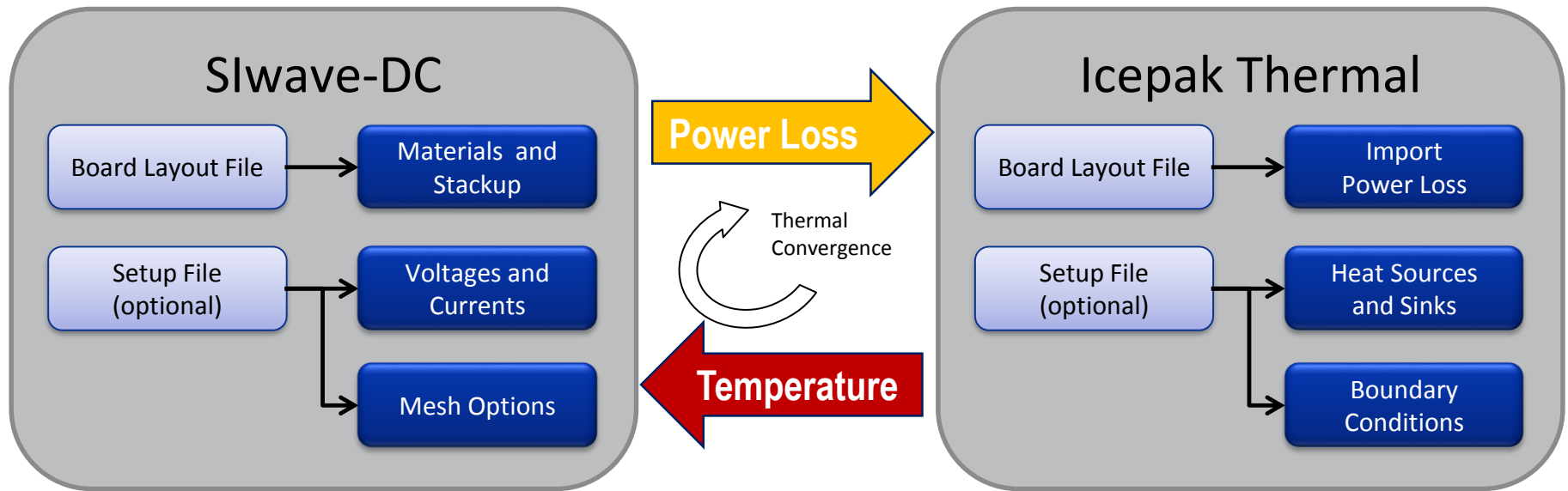
Overview: SIwave-DC Automated Report

Fully Automated Report:

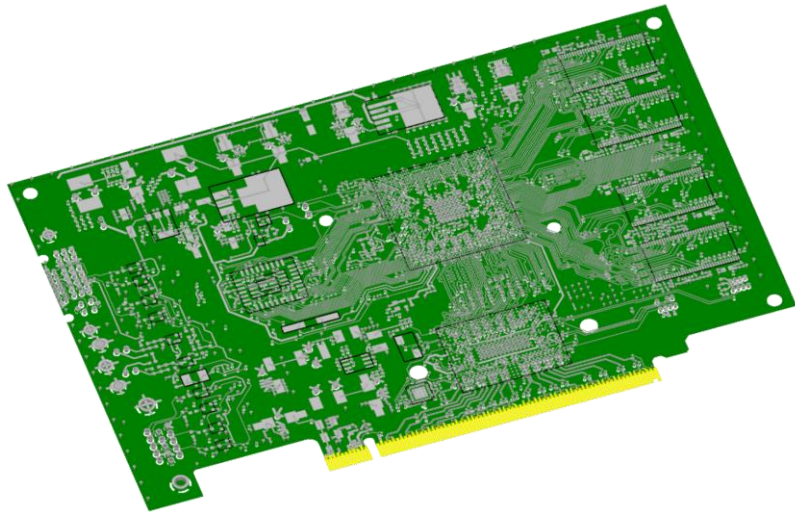
- Set Voltage/Current Limits
- HTML or PDF Format
- Layer by Layer Results



Overview: SIwave-DC with Icepak (not covered today)



Thermal Solutions: Slwave-DC with Icepak

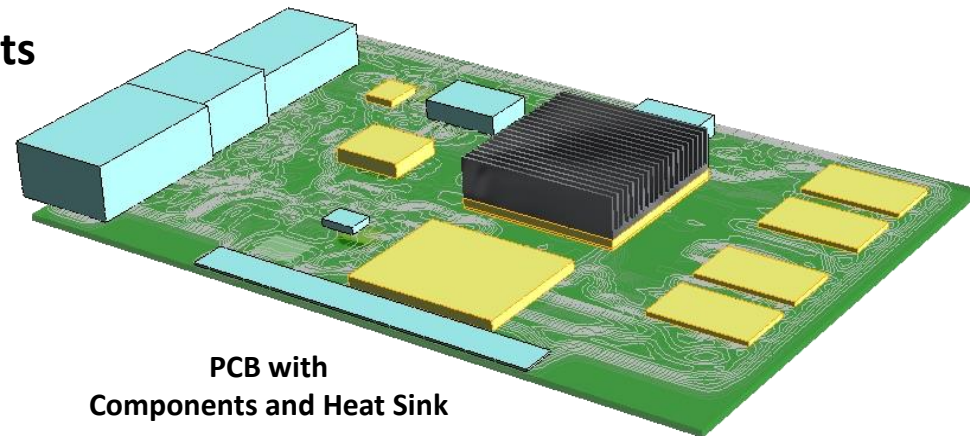
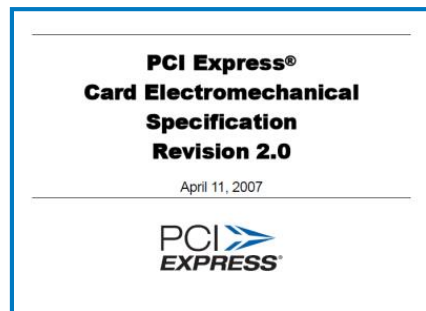


| Impact of Slwave & Icepak Link | DC Power Consumption |
|--------------------------------|----------------------|
| Without Joule Heating | 69.3 Watts |
| With Joule Heating | 75.7 Watts |

Max power not to exceed 75 W

PCI Express Specification:

- Includes dissipation from active components and conduction Joule heating.

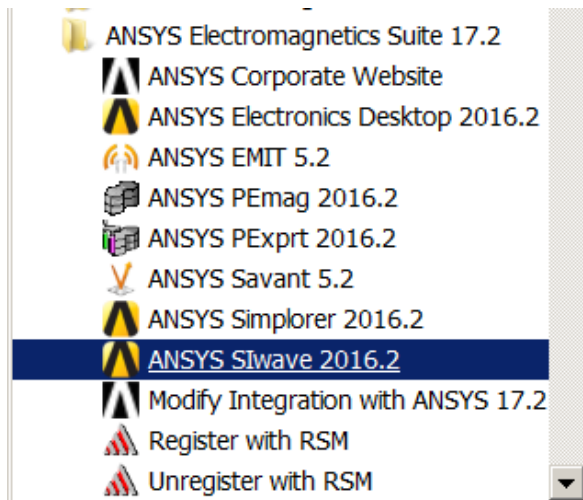


PCB with
Components and Heat Sink

Opening or Importing a Project

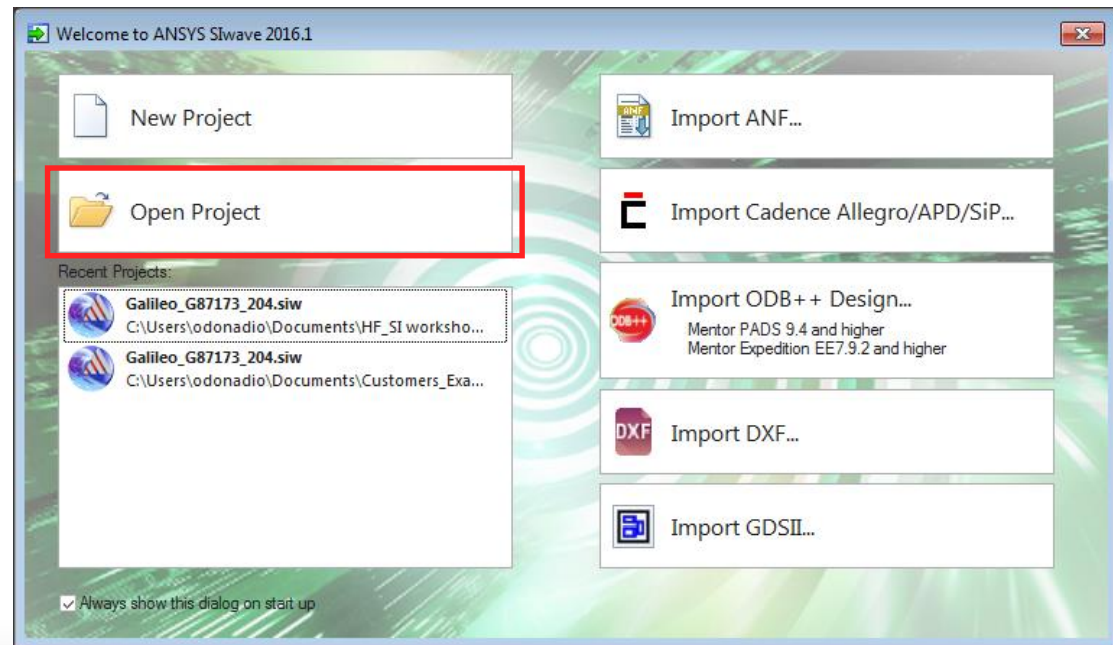
Starting SIwave

- To launch SIwave, click the Microsoft **Start** Button > **ALL Programs** > **ANSYS Electromagnetics** > **ANSYS Electromagnetics Suite 17.2**.
- Select the **ANSYS SIwave 2016.2** executable.



Open a SIwave Project

- Select the **Open Project** button
 - Browse for the file: **Galileo_G87173_204.siw**
 - Click the **Open** button



SIwave v2016.1 Workspaces

Common Functions

Component Control

GUI Style Selector

Menu Ribbon

Net Control

Layer Visibility Control

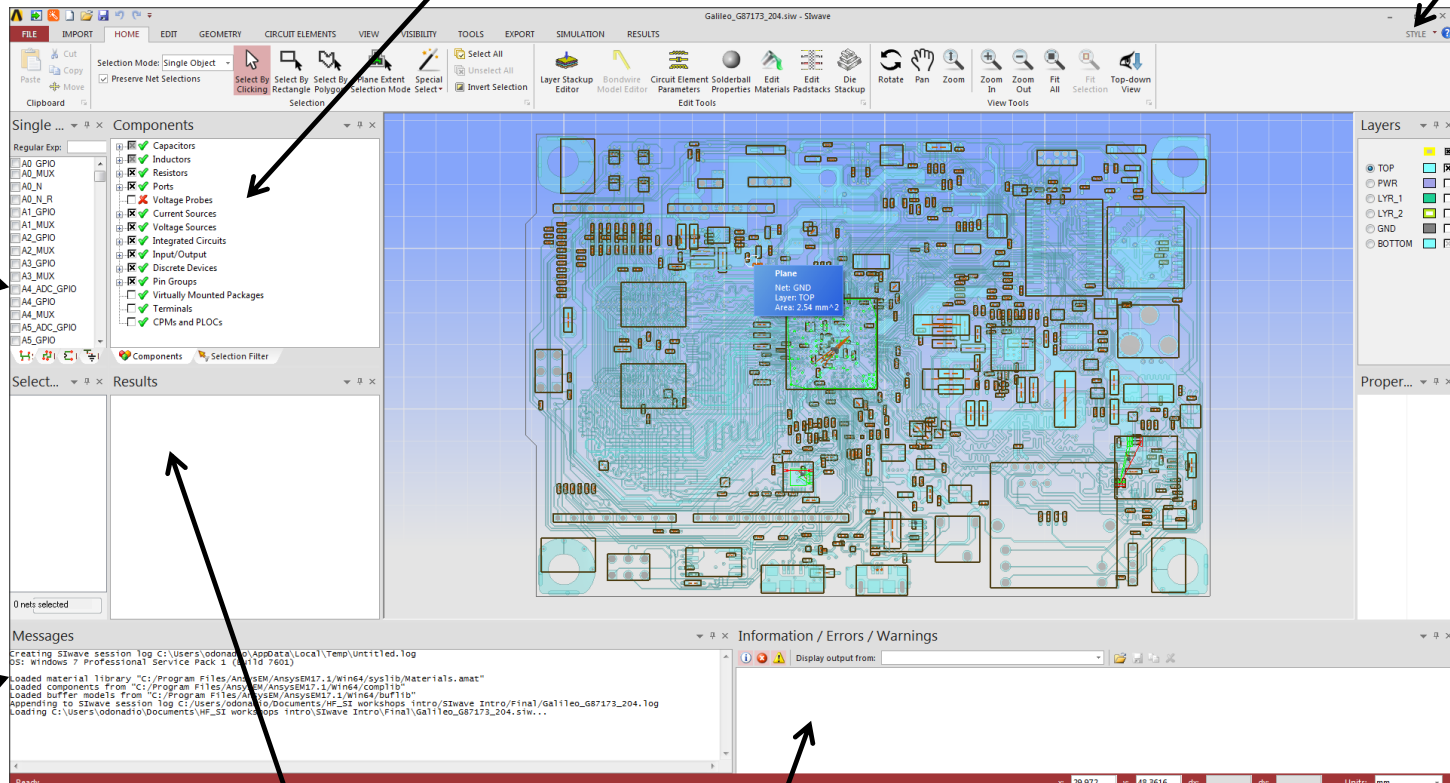
Selected Properties

Process Messages

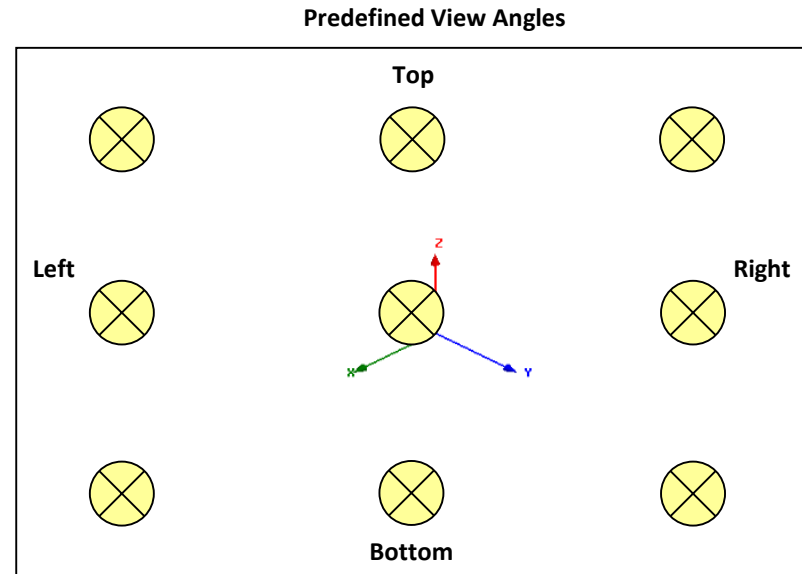
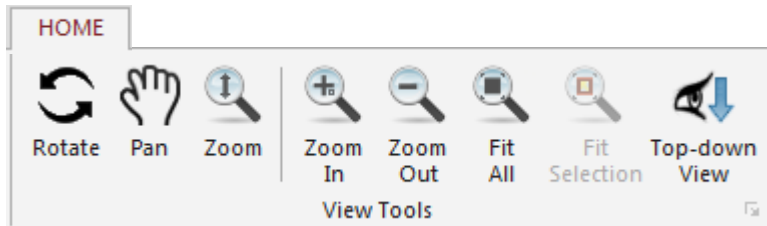
Results Selection

Alerts

Coordinates and Global Units



Changing the View



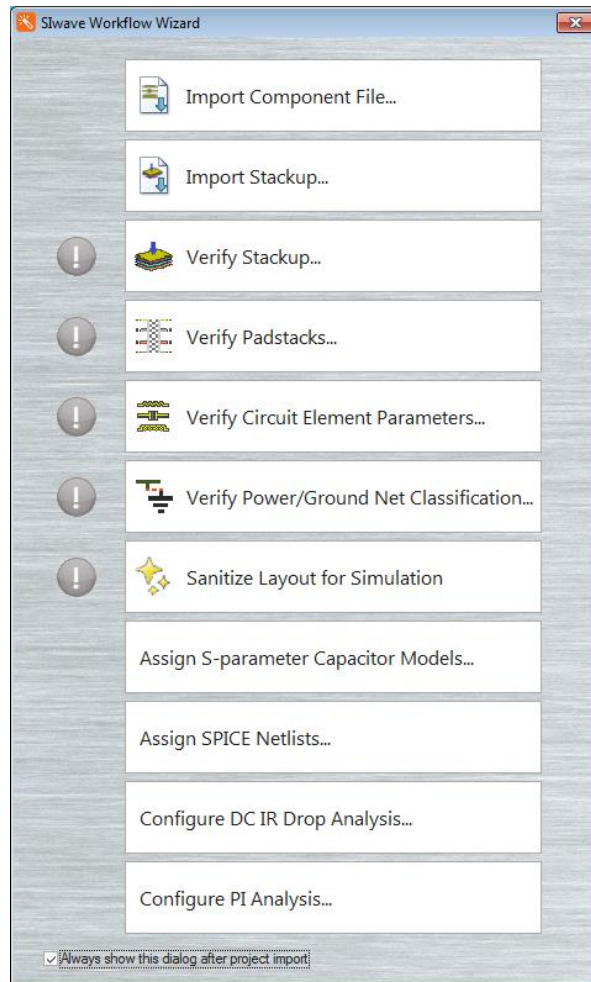
– Shortcuts

- Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:
 - Fit All: **Ctrl + D**
 - Rotate: **ALT + Drag** or **Click Left Mouse Button + Drag**
 - In addition, there are 9 pre-defined view angles that can be selected by holding the **ALT** key and double clicking on the locations shown on the next page.
 - Pan: **Shift + Drag**
 - Dynamic Zoom: **ALT + Shift + Drag** or **Mouse Wheel**

SIwave Workflow Wizard Dialogue

- **Opening the Workflow Wizard**

- In the Common Functions menu, choose the **SIwave Workflow Wizard Dialogue**.



(Optional) Import Settings
from Previous Simulation

**Verify / Modify Geometry,
Materials, and Circuit Elements**

(Optional) Pre-process Overlapping Geometry

(Optional) Assign Broadband Models

Setup Simulation

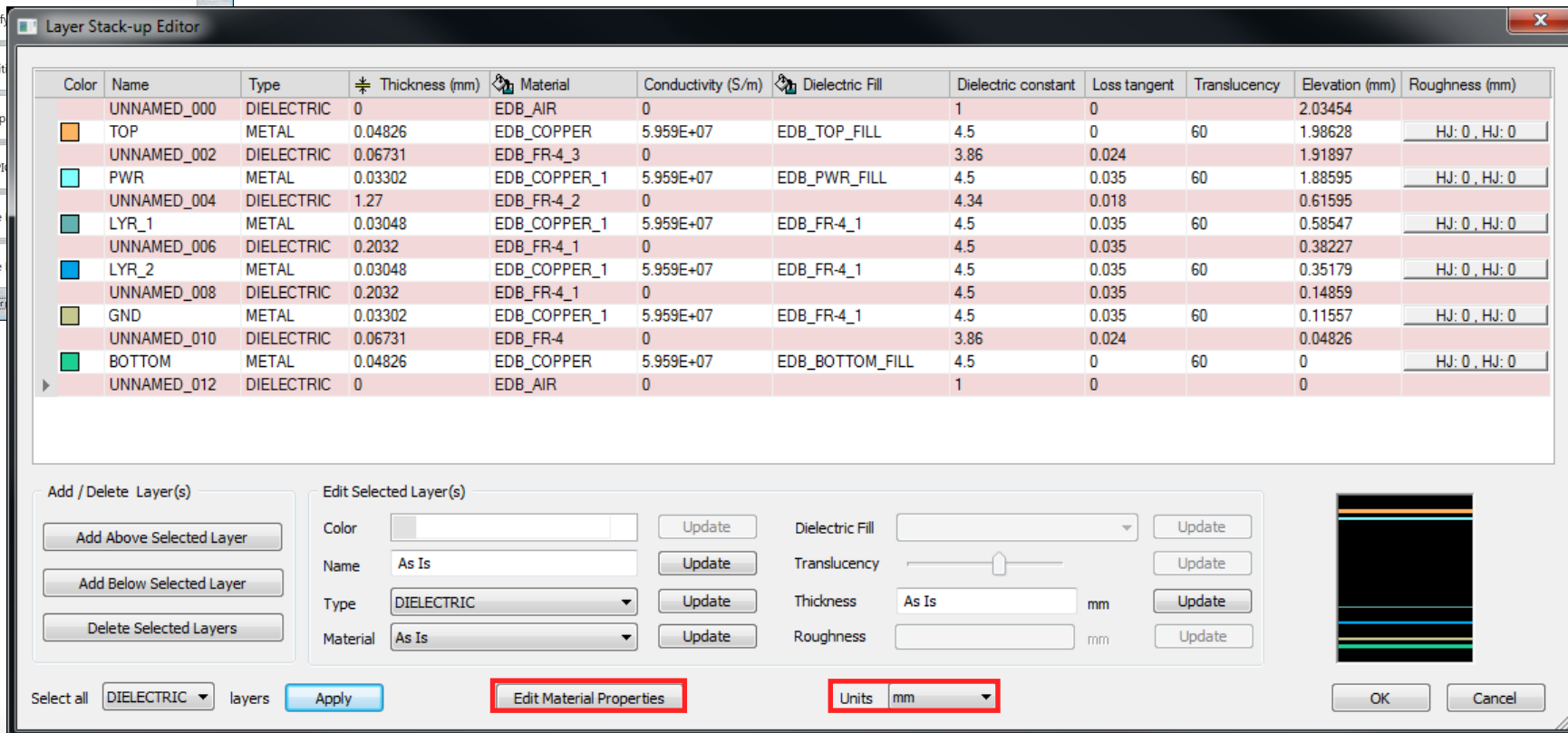
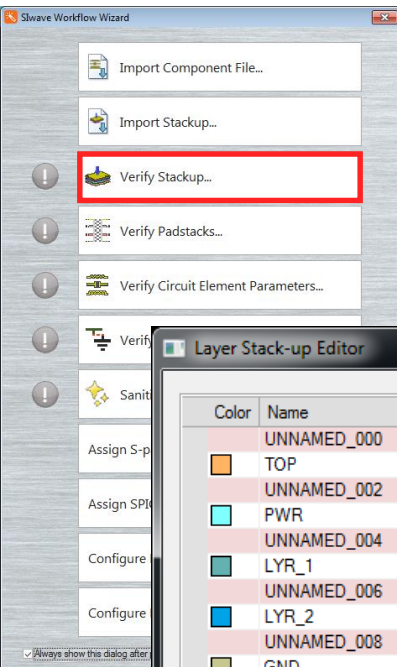
Verify Stackup

- **Modify Stackup and Material Properties**

- Click on the **Verify Stackup** button

- Change the **Units** to **mils** by using the drop down box. Observe the change in the Thickness column.

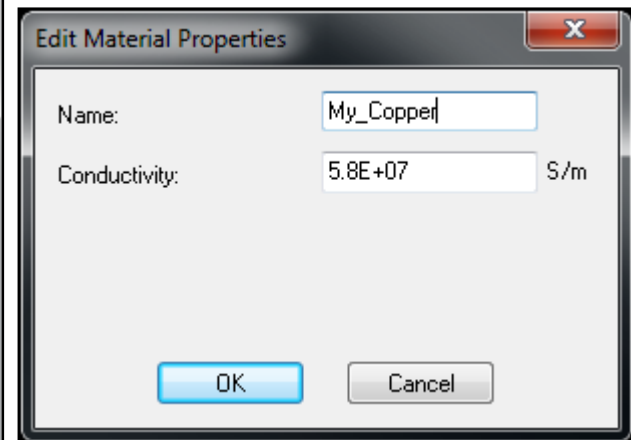
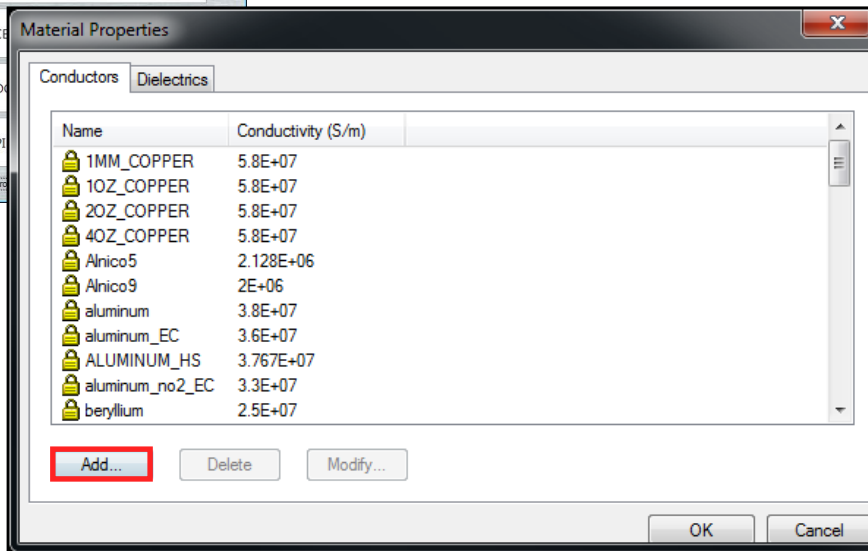
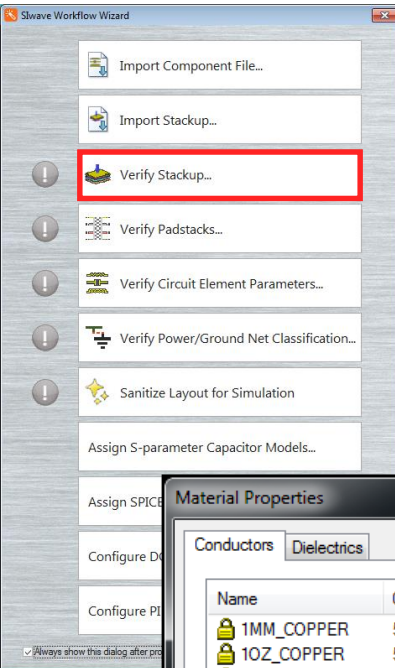
- Click on the **Edit Material Properties** button to open the **Material Properties** window.



Verify Stackup, cont.

- **Add a New Conductor**

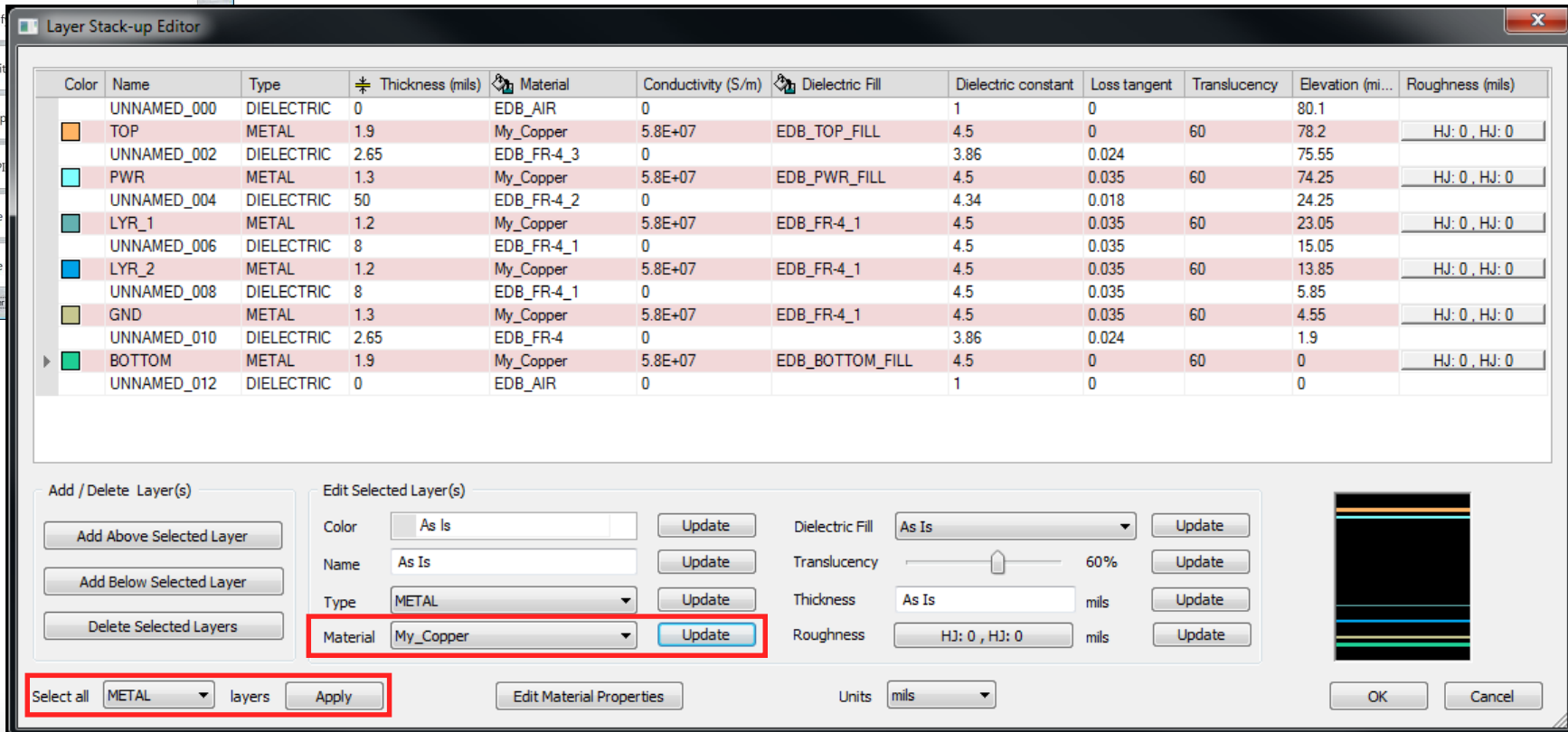
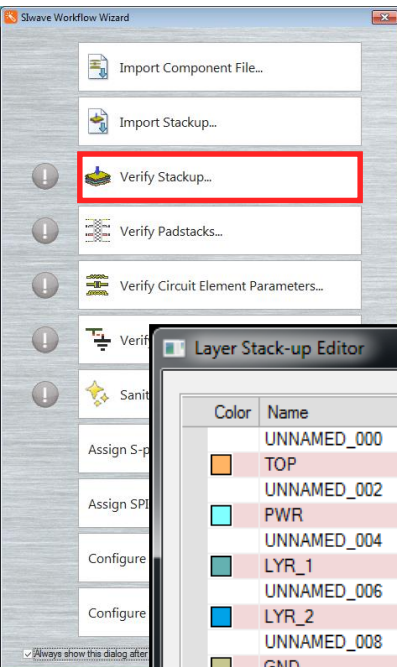
- Select the **Conductors** tab if it is not already selected.
- Click the **Add** button to add a new material.
- Edit the properties.
 - Name: **My_Copper**
 - Conductivity: **5.8E+07 S/m**.
- Click **OK** to close the Edit Material Properties window.
- Click **OK** to close the Material Properties window.
- A warning will appear about committing changes. Press the **Yes** button to continue.



Verify Stackup, cont.

- **Modify Project Materials**

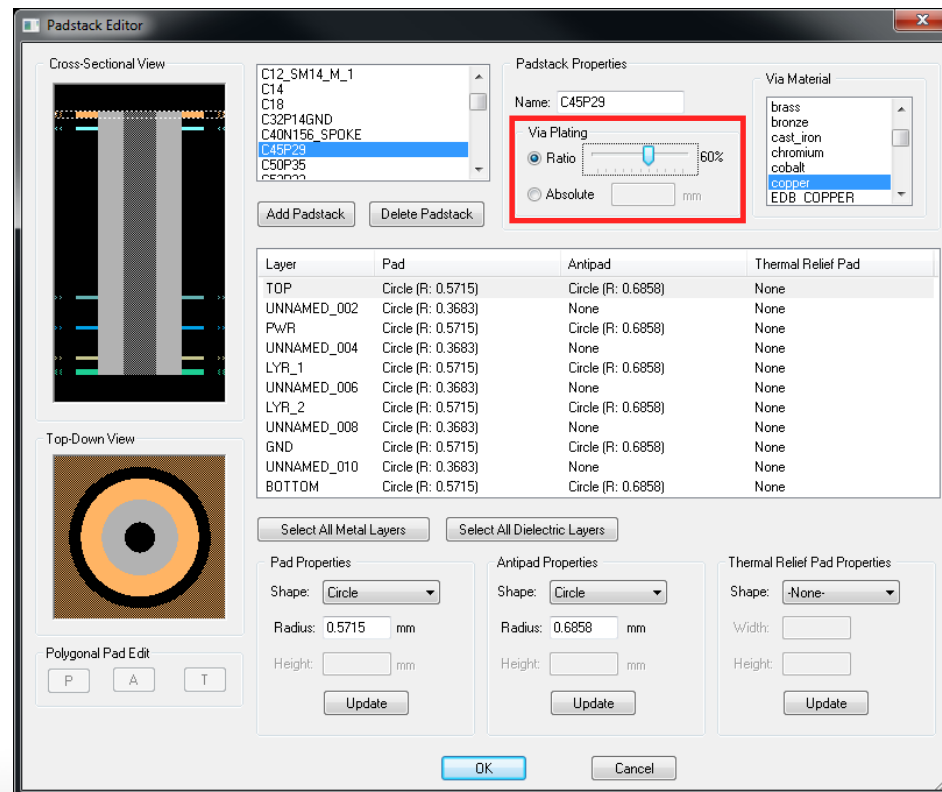
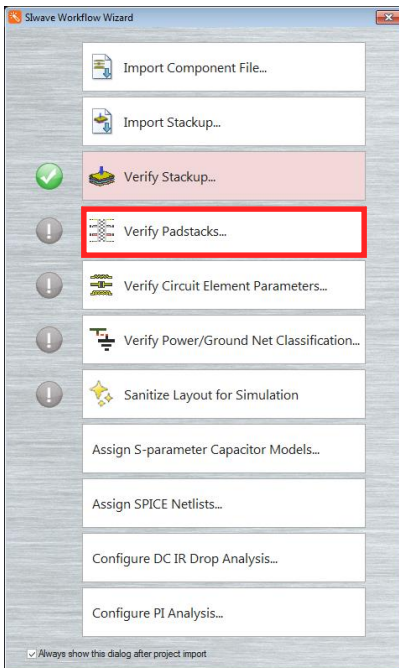
- Using the drop down box at the bottom, choose **METAL** and click the **Apply** button.
- Change the Material field to **My_Copper** and click the **Update** button.
- Click **Cancel** to not commit changes and close the Layer Stack-up Editor.



Verify Padstacks

- **Modify Padstack Definitions**

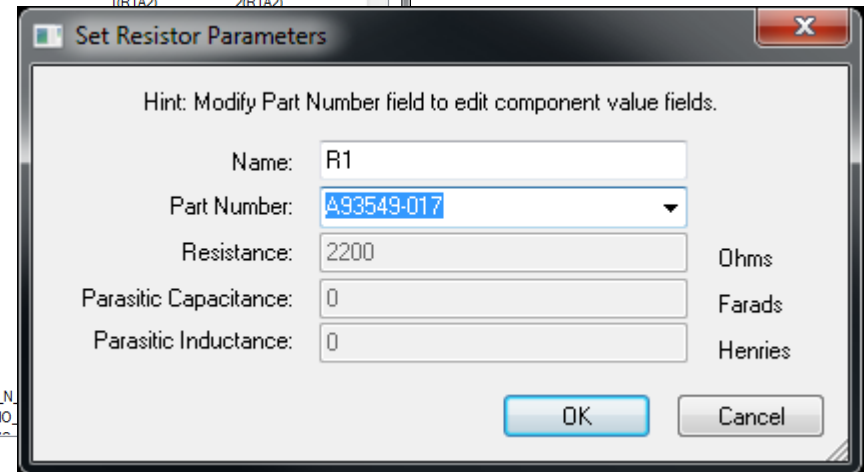
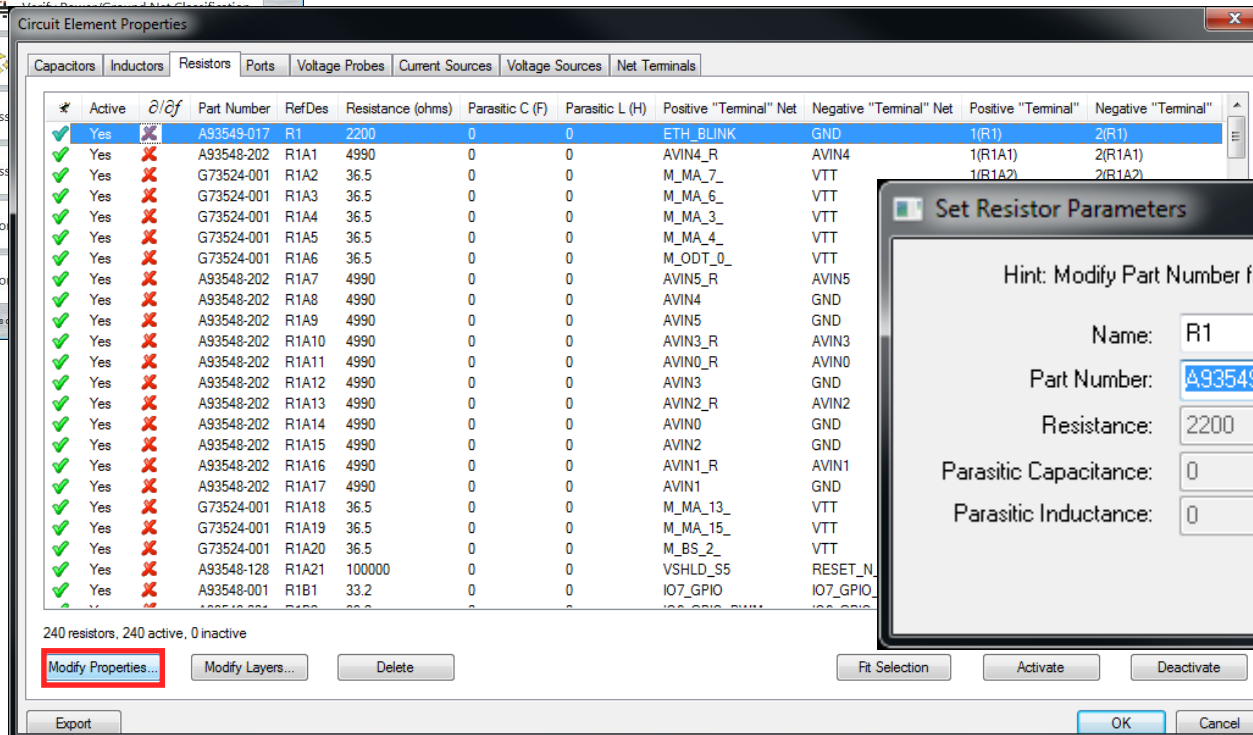
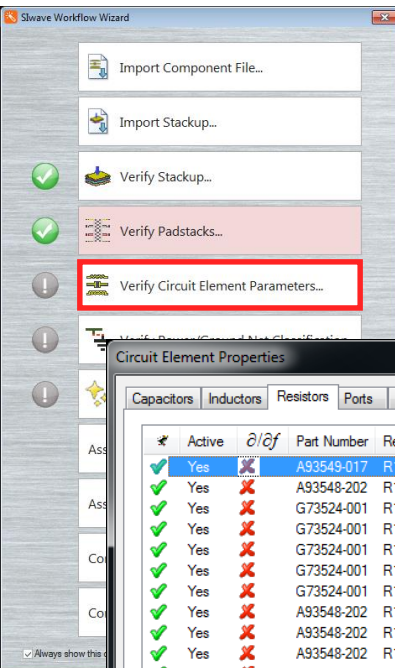
- Click on the **Verify Padstacks** button to open the Padstack Editor.
- Via plating determines the amount of conductor plated up inside of a via.
- Choose a padstack and change the **Ratio** percentage by adjusting the slider bar.
- Siwave defaults all via plating to 100% fill for all padstacks.
- Selecting **Absolute** instead of **Ratio** will give you the wall thickness in the current units and vice versa.
- Click **Cancel** to not commit the changes and close the Padstack Editor window.



Verify Circuit Element Parameters

• Modify Circuit Elements

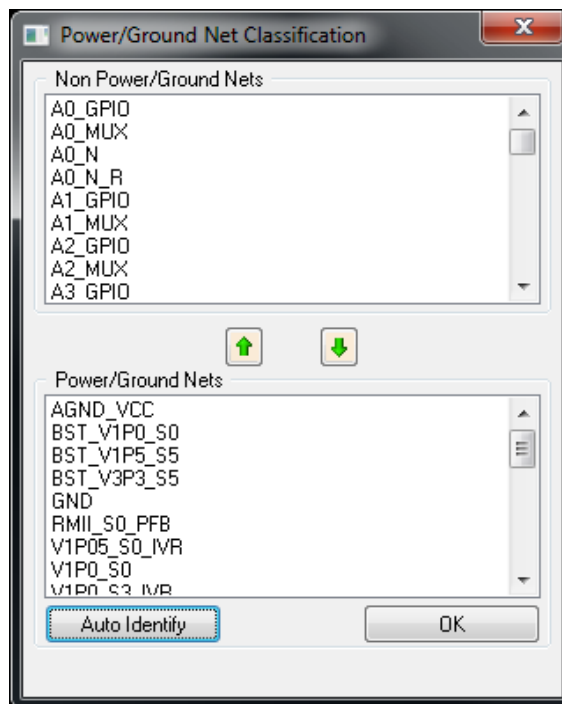
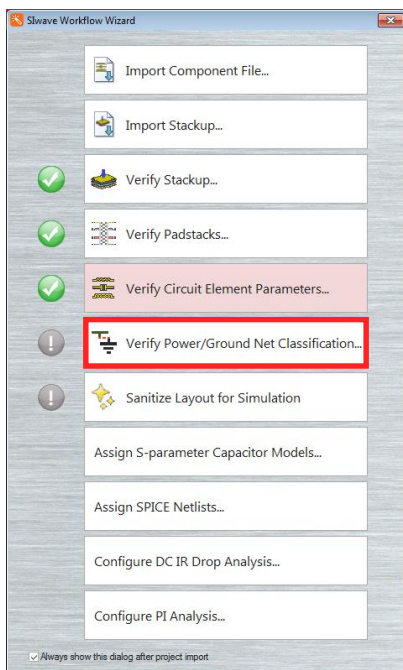
- Click on the Verify Circuit Element Parameters button to open the Circuit Element Properties window.
- Inductors and Resistors are important for DC operation. Verify they have been imported properly.
- Choose the first resistor named R1 and click the **Modify Properties** button.
- In the Set Resistor Parameters window, you can change the name or the associated Part Number.
- Click **Cancel** to close the Set Resistor Parameters window.
- Click **Cancel** to close the Circuit Element Properties window.



Verify Power/Ground Net Classification

- **Modify Power/Ground Net Classification**

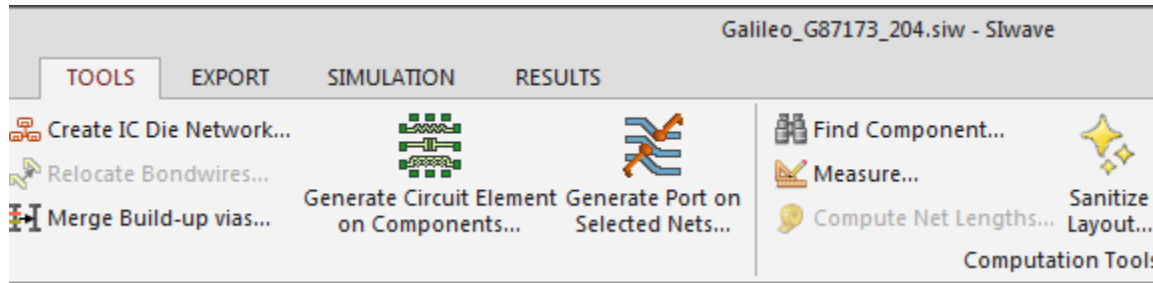
- Click on the **Verify Power/Ground Net Classification** button.
- SIwave automatically determines that any net with defined with polygons or shapes as power/ground.
- SIwave does not automatically classify nets with only traces and padstacks as power/ground.
- Move nets in and out of the classification by using the up/down arrows.
- Click on **Auto Identify** to bring the classification back to default.
- Click **OK** to close the window.



Sanitize Layout

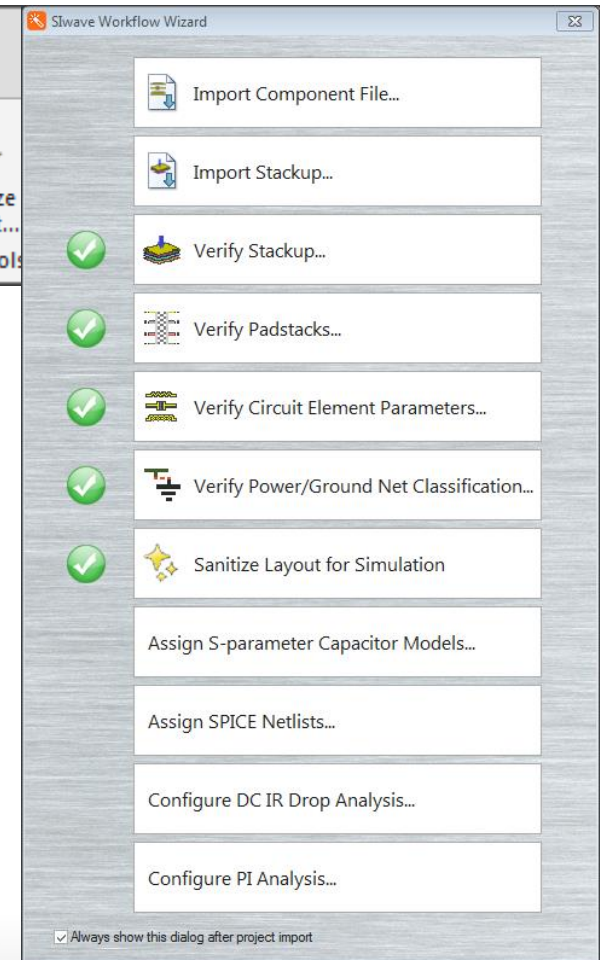
Cleans up ECAD Geometry

- Results in Higher Simulation Success Rate
- Speeds up Solver and Reduces RAM usage



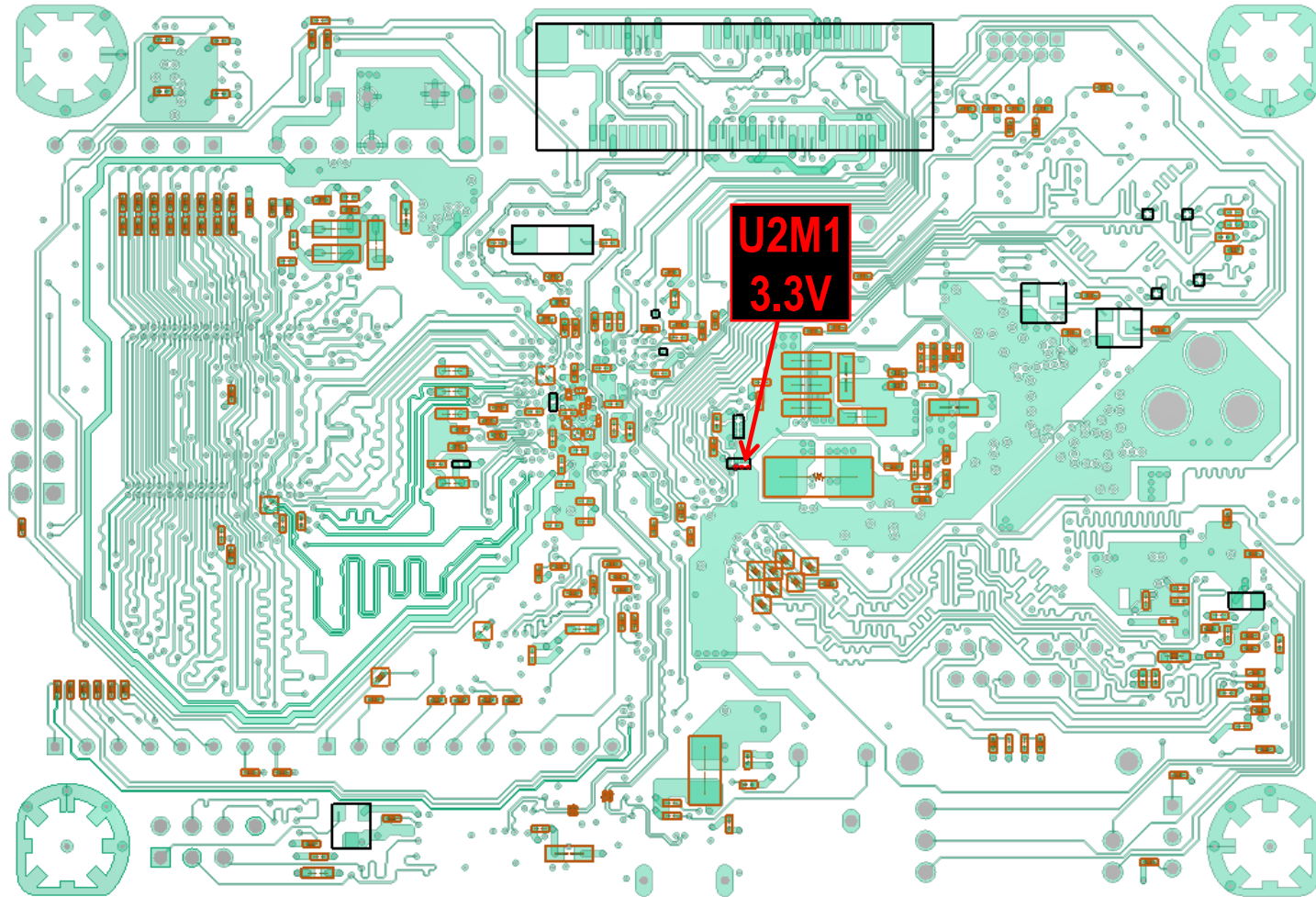
Heuristically ensures nets identified as PWR/GND have:

- Planes defined as Planes
- Traces defined as Traces
- Overlapping Traces or Traces within Traces are cleaned up

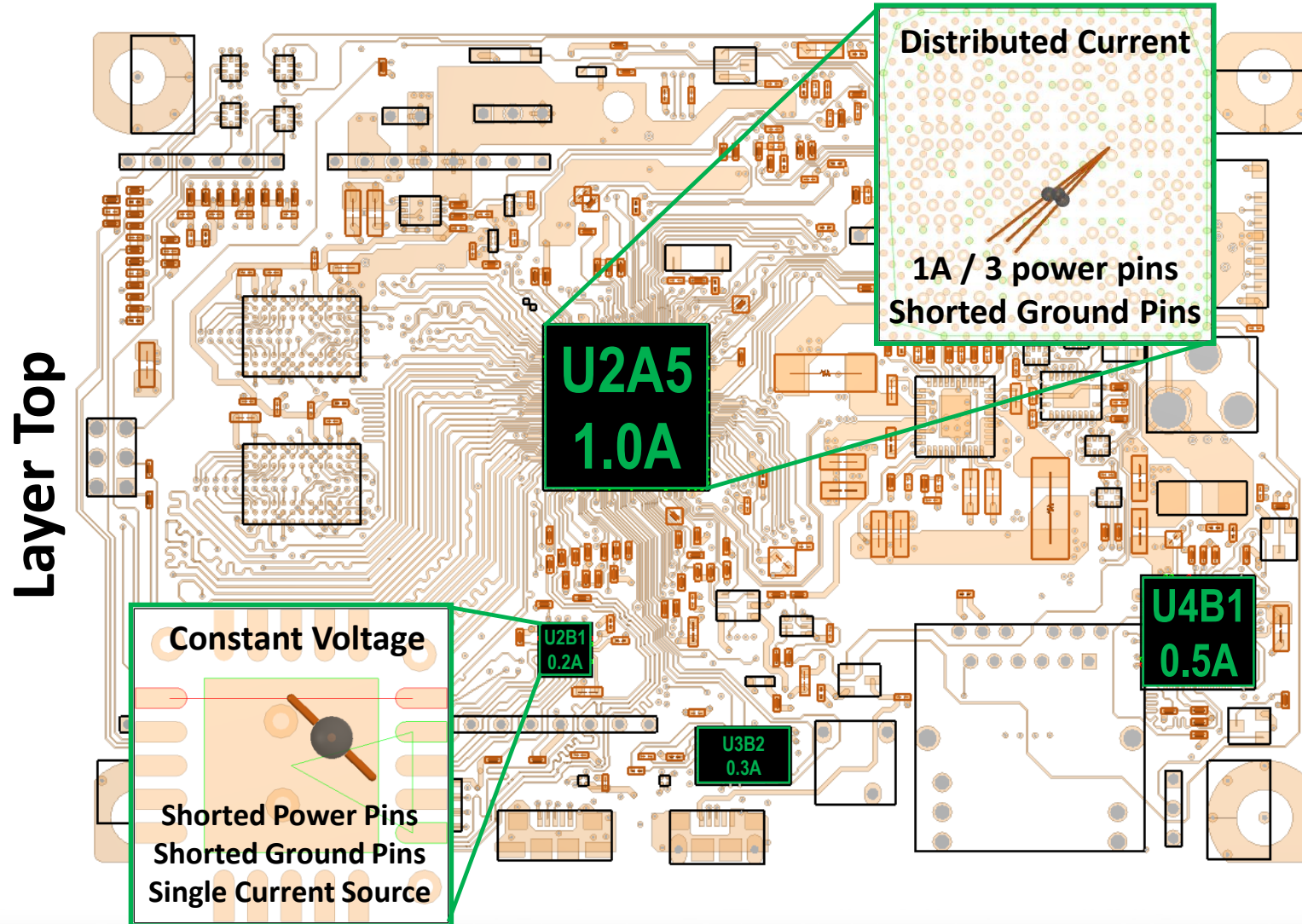


DC IR Simulation Excitations

Layer Bottom



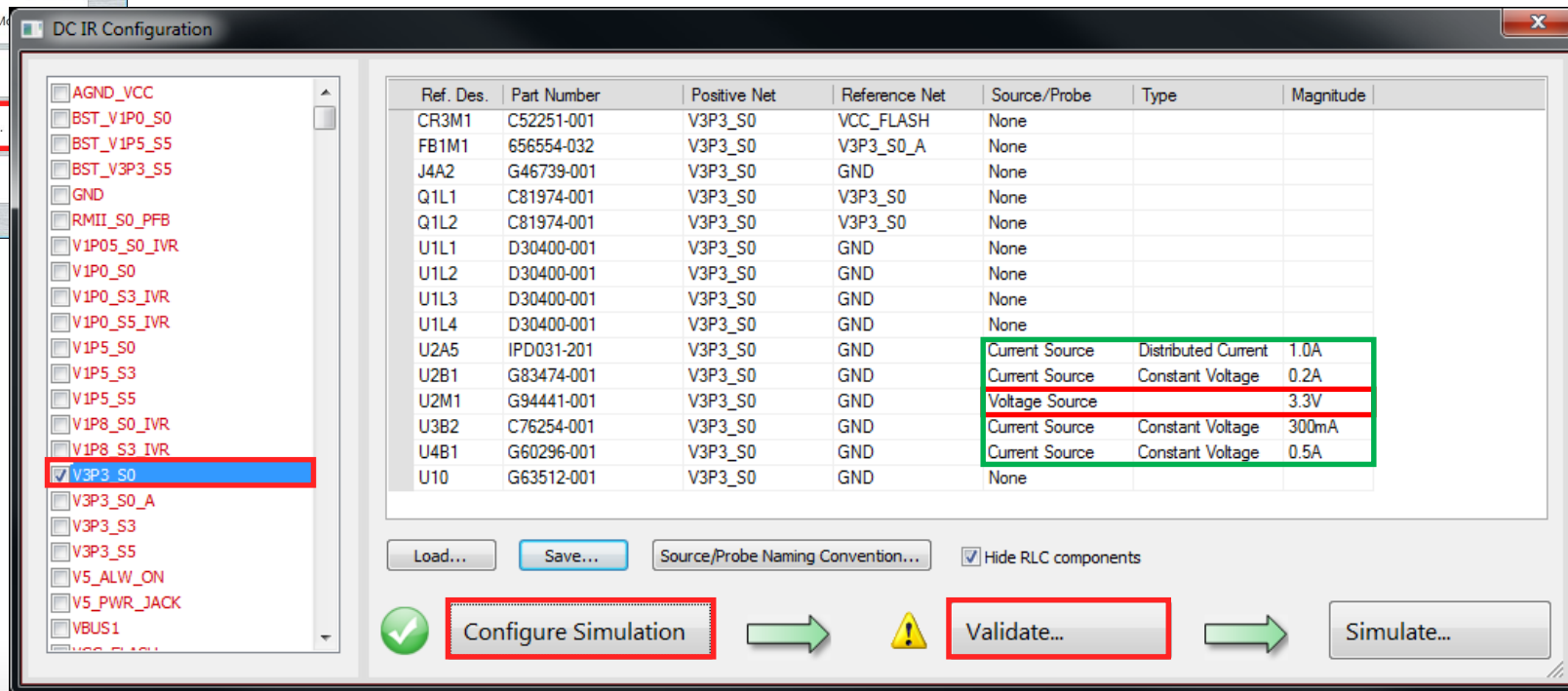
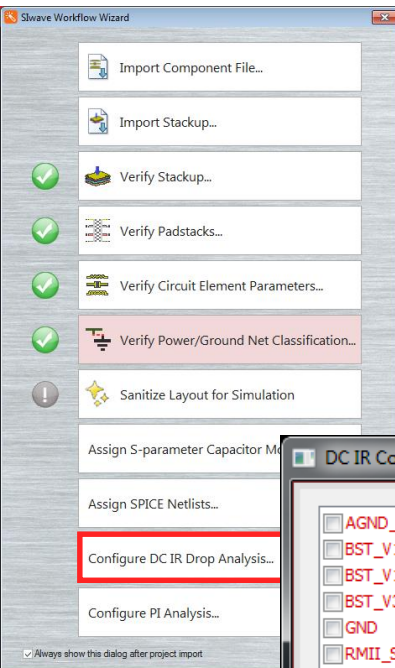
DC IR Simulation Excitations



Configure DC IR Drop Analysis

- **Table Driven Schematic**

- Place a check mark next to net **V3P3_S0**.
 - This displays any active devices connected to this net.
 - Check and uncheck **Hide RLC components** to see passive devices.
- Set **current and voltage sources** as shown in the graphic below.
- Click the **Save** button to save a flow configuration file (.fcf).
 - This can be loaded for subsequent simulations.
- Click the **Configure Simulation** button to apply pin groups and excitations to the design.
- Click the **Validate** button.



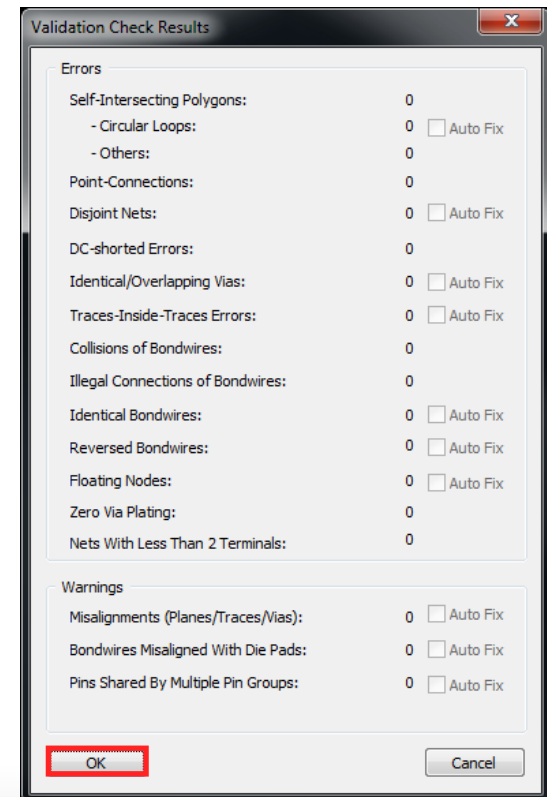
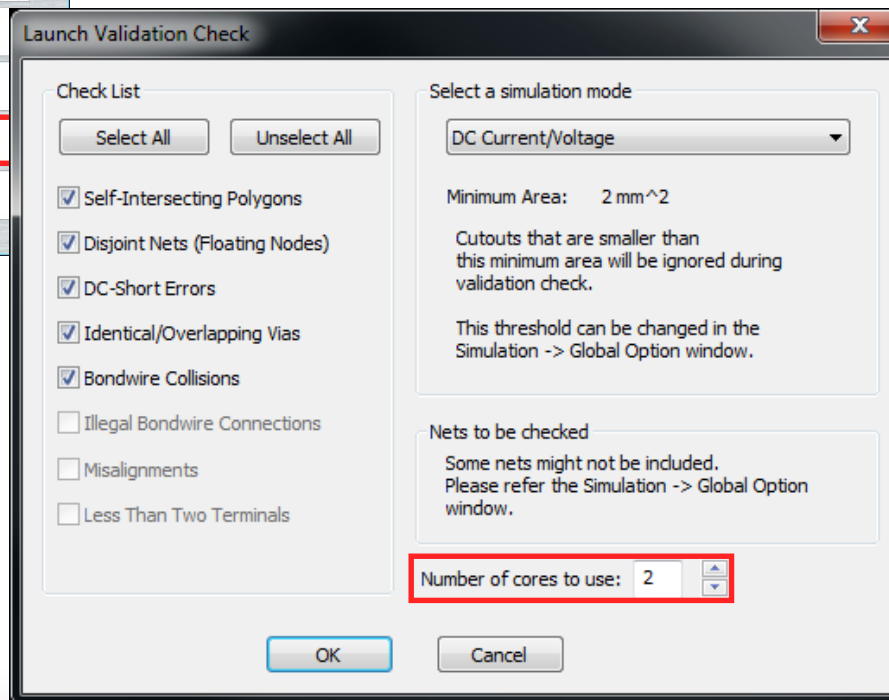
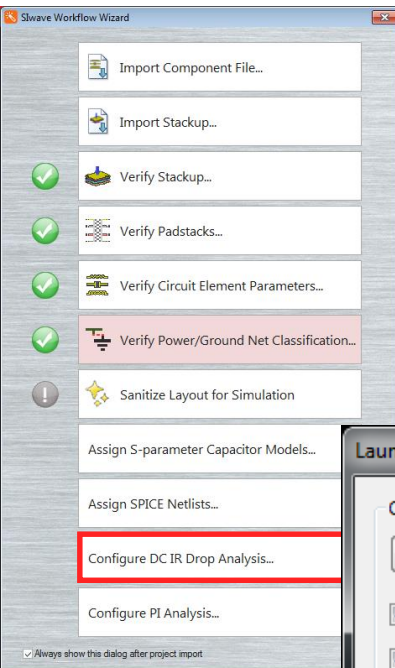
Validation Check

- **Validation Check**

- The validation check analyzes the entire setup to ensure it is ready for simulation.
- Increase the **Number of cores to use** for this validation step by pressing the up button.
- Click **OK** to start the validation check.

- **Validation Check Results**

- The Validation Check can automatically repair certain geometry problems such as disjoint nets and overlapping vias.
- Press **OK** to apply any Auto Fix and to close this window.



Configure DC IR Drop Analysis, cont.

- **Simulation**

- Closing the Validation Check returns you to the DC IR Configuration window.
- Click the **Simulate...** button.

The screenshot shows the ANSYS SIWave Workflow Wizard on the left and the DC IR Configuration dialog on the right. The wizard has several steps, with 'Configure DC IR Drop Analysis...' highlighted in red. The DC IR Configuration dialog shows a list of components on the left and a table of simulation results on the right. The 'Simulate...' button is highlighted in red.

DC IR Configuration

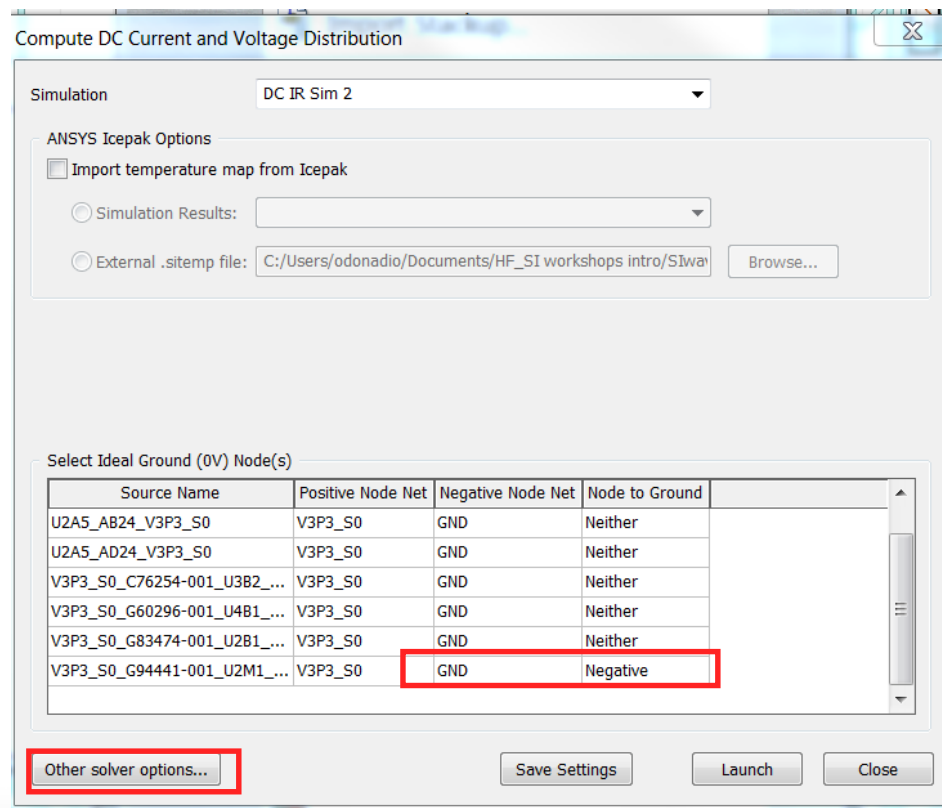
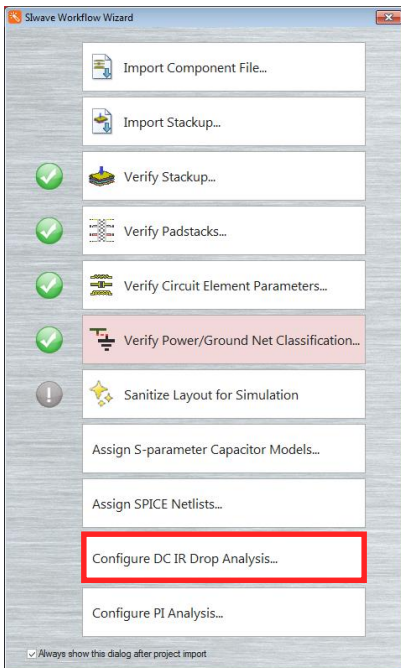
| Ref. Des. | Part Number | Positive Net | Reference Net | Source/Probe | Type | Magnitude |
|-----------|-------------|--------------|---------------|----------------|---------------------|-----------|
| CR3M1 | C52251-001 | V3P3_S0 | VCC_FLASH | None | | |
| FB1M1 | 656554-032 | V3P3_S0 | V3P3_S0_A | None | | |
| J4A2 | G46739-001 | V3P3_S0 | GND | None | | |
| Q1L1 | C81974-001 | V3P3_S0 | V3P3_S0 | None | | |
| Q1L2 | C81974-001 | V3P3_S0 | V3P3_S0 | None | | |
| U1L1 | D30400-001 | V3P3_S0 | GND | None | | |
| U1L2 | D30400-001 | V3P3_S0 | GND | None | | |
| U1L3 | D30400-001 | V3P3_S0 | GND | None | | |
| U1L4 | D30400-001 | V3P3_S0 | GND | None | | |
| U2A5 | IPD031-201 | V3P3_S0 | GND | Current Source | Distributed Current | 1A |
| U2B1 | G83474-001 | V3P3_S0 | GND | Current Source | Constant Voltage | 0.2A |
| U2M1 | G94441-001 | V3P3_S0 | GND | Voltage Source | | 3.3V |
| U3B2 | C76254-001 | V3P3_S0 | GND | Current Source | Constant Voltage | 300mA |
| U4B1 | G60296-001 | V3P3_S0 | GND | Current Source | Constant Voltage | 0.5A |
| U10 | G63512-001 | V3P3_S0 | GND | None | | |

Buttons: Load..., Save..., Source/Probe Naming Convention..., Hide RLC components (checked), Configure Simulation, Validate..., Simulate...

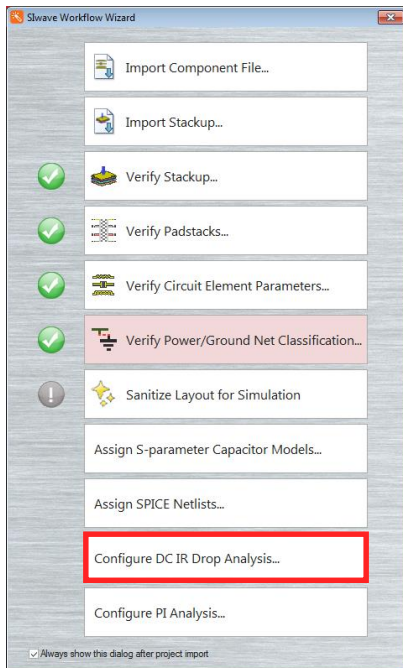
Launching the DC IR Simulation

- **Compute DC Current and Voltage Distribution**

- Siwave requires a global 0 Volt reference location. It is automatically applied to the negative pin of the voltage source. This creates a reference point for voltage plots in the results.
- Change the **Simulation name** to **DC IR Sim 1** if it is not already set.
- Click the **Other solver options...** button.

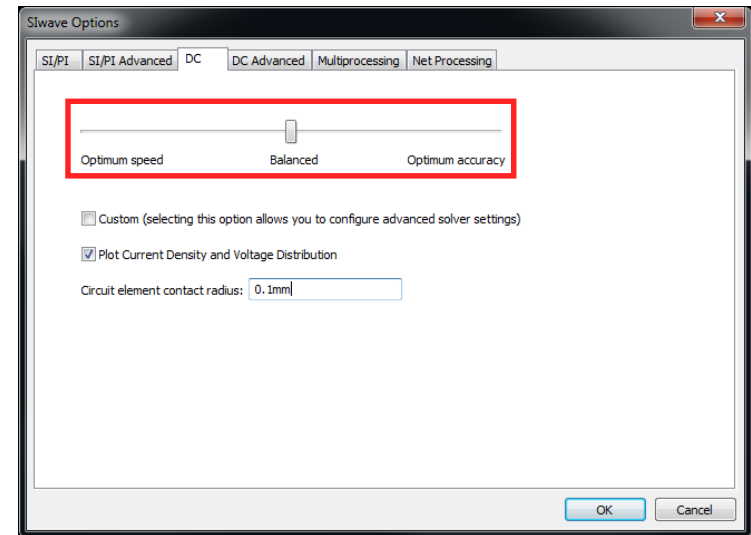


Launching the DC Simulation, cont.

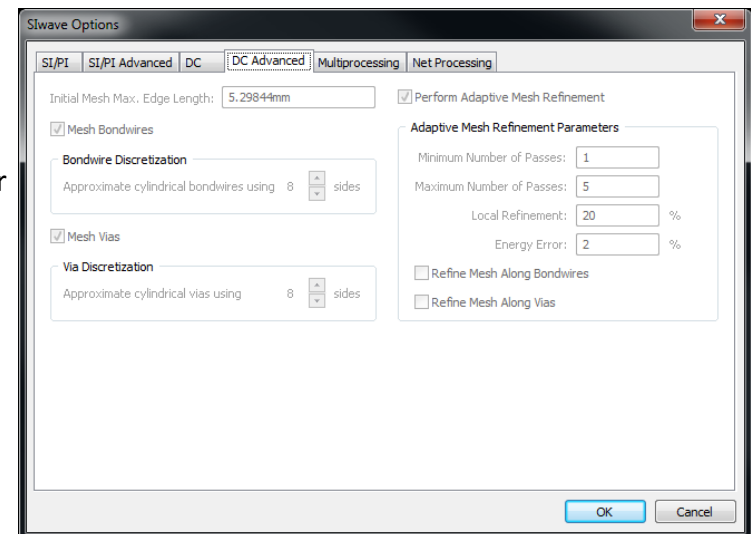


- **SIwave Options**

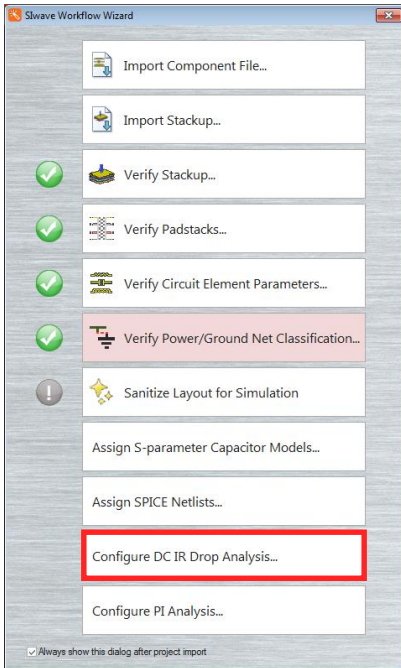
- DC tab
 - Choose **Balanced**
 - The slider bar allows you to choose between three predefined settings. To see what settings are changed, move the slider bar to different positions and click on the DC Advanced tab.



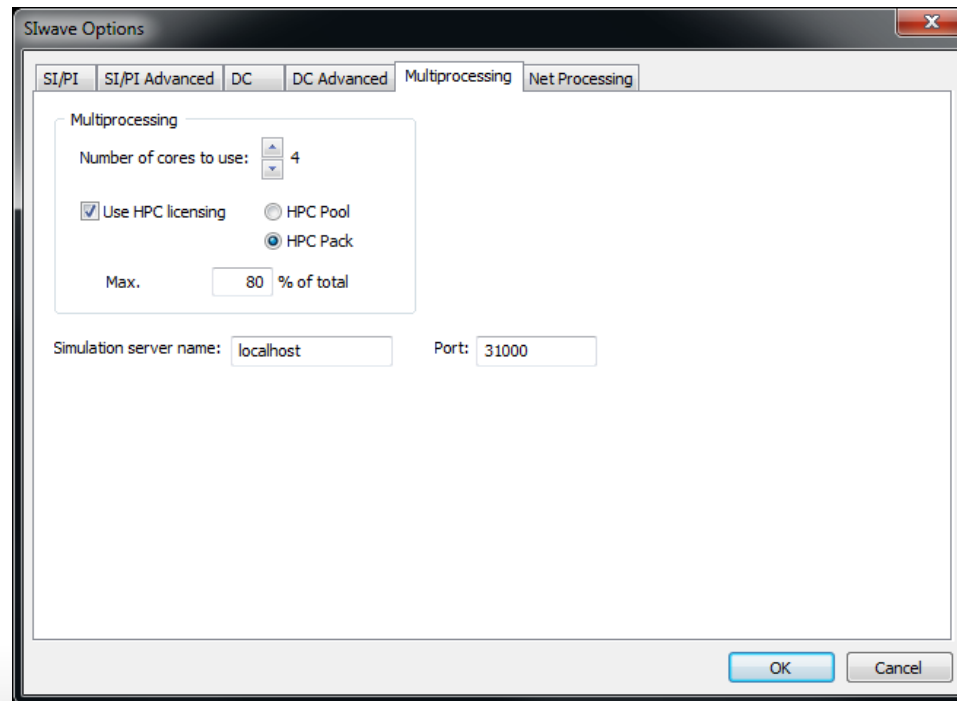
- DC Advanced tab
 - Note that we are Meshing vias and performing adaptive mesh refinement for planes and traces.



Launching the DC IR Simulation, cont.

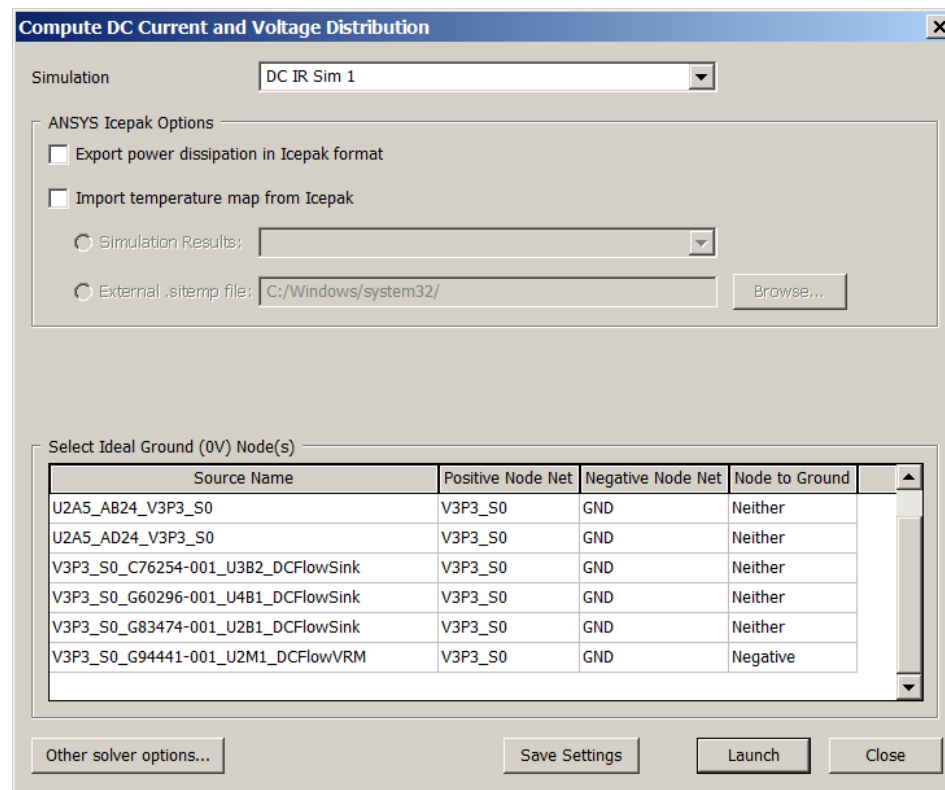
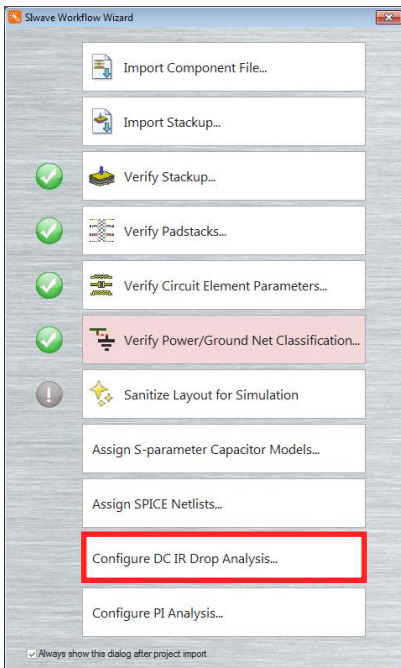


- **Multiprocessing (High Performance Computing, HPC)**
 - For a DC simulation, HPC can distribute the solver across multiple cores.
 - Click on the **Multiprocessing** tab.
 - Ensure the following options are set:
 - Number of cores to use: **Max** (increase until it stops incrementing)
 - Use HPC Licensing: **Enable**
 - HPC Pack: **Selected**
 - Max: 80% of total RAM
 - Click **OK** to close this window.



Launching the DC IR Simulation, cont.

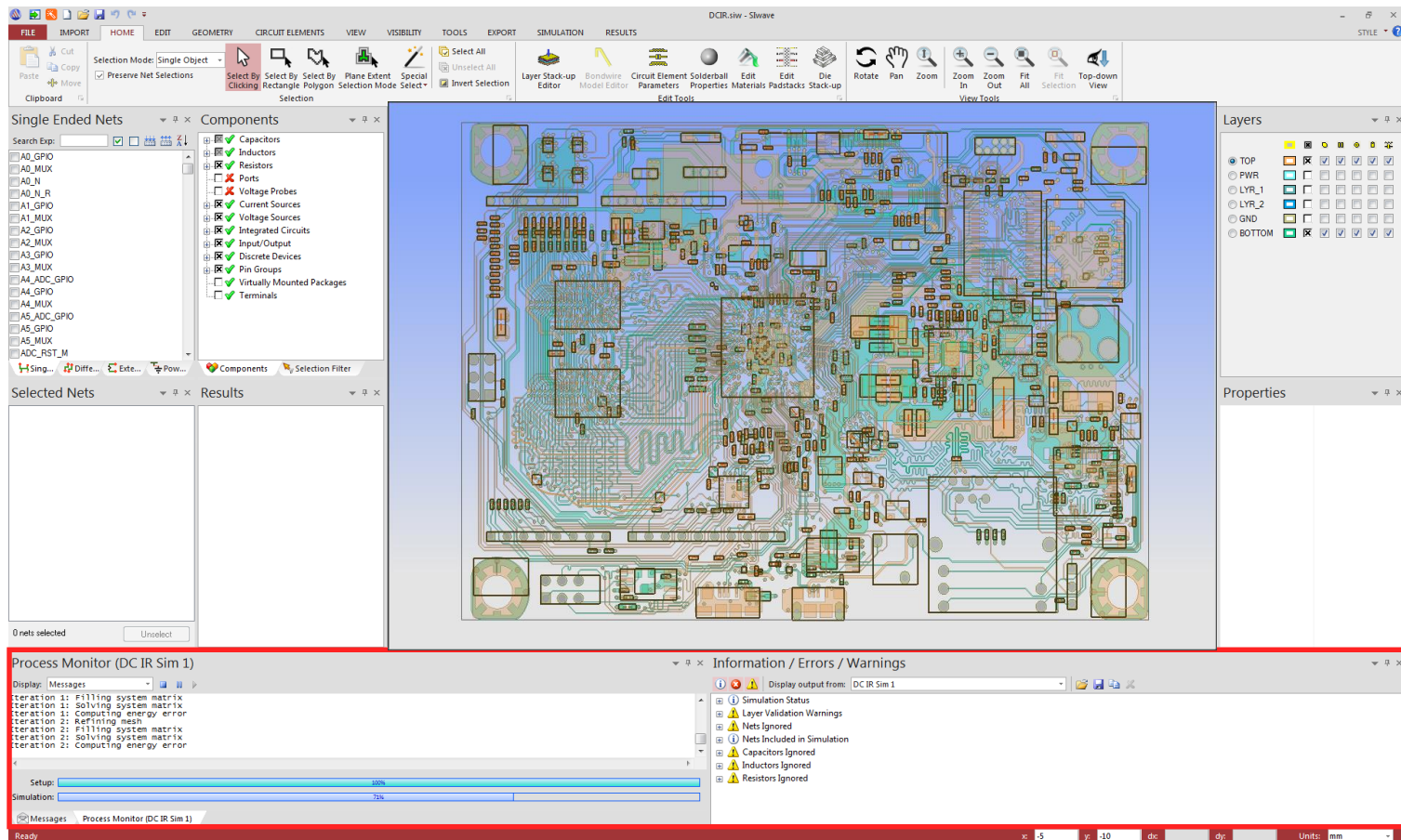
- **Begin the DC IR Simulation**
 - Click the **Launch** button.



DC Simulation Status

- **Process Monitor and Information / Errors / Warnings**

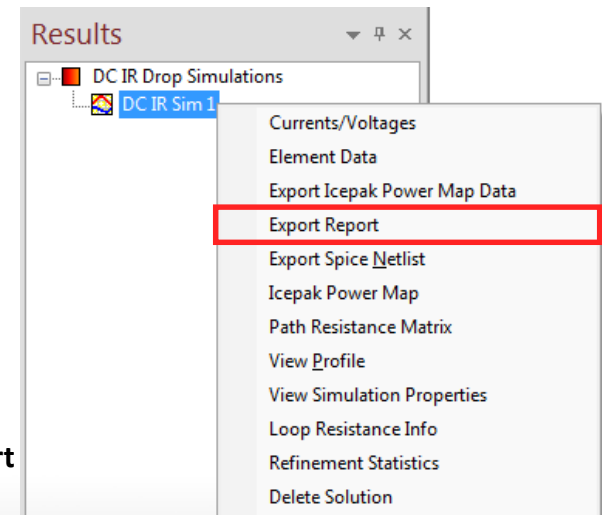
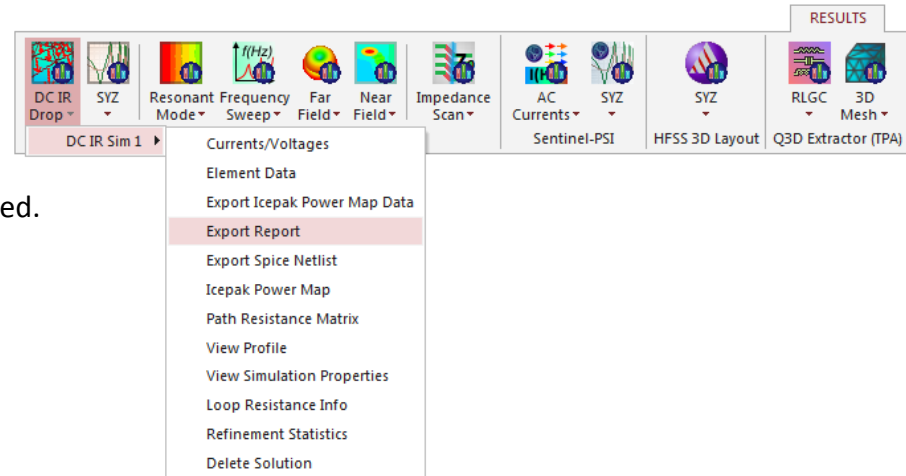
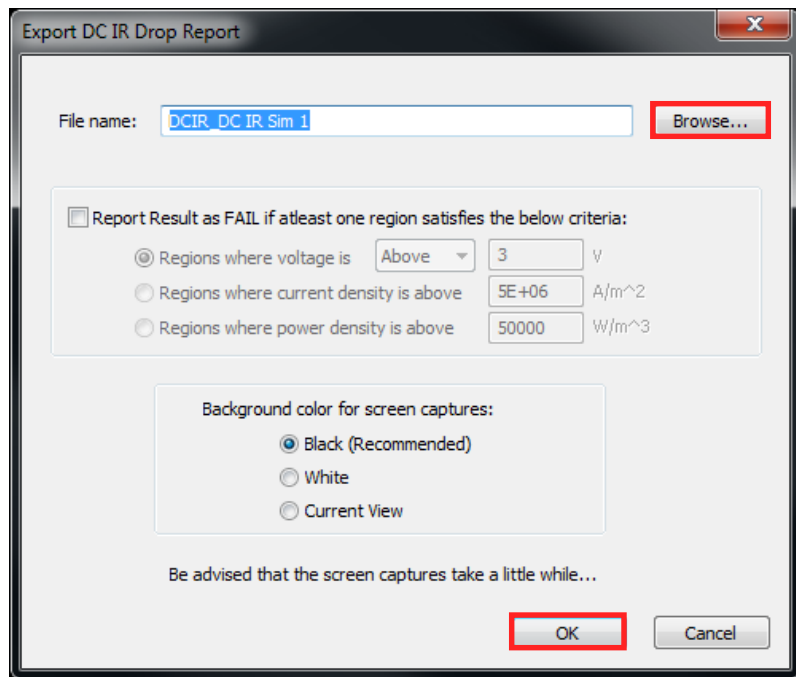
- The process monitor shows the simulation status and steps taken by the solver.
- Information / Errors / Warnings alerts you to any potential issues that may arise during the solution process.



DC Simulation Results: Automated Report

- **Exporting the Automatic Report**

- From the Results menu, choose:
 - **DC IR Drop > DC IR Sim 1 > Export Report**
- Click on the **Browse** button to specify a file location.
- Click **OK**. **DCIR_DC IR Sim 1.htm** and associated files will be created.
- Please be patient. Slwave is actively taking screen captures.



- Alternatively, from the results window:
 - **Right-click DC IR Sim 1 > Export Report**

DC Simulation Results: Automated Report

• Open the Report in a Web Browser

- Open the .htm file using your favorite browser. [DCIR_DC IR Sim 1.htm](#)
- Stackup and Setup information are contained in the header section.
- Layer by layer results are captured here for Current Density, Voltage, and Power Loss.
- Plots can be resorted by layer or plot type by clicking the hyperlink indicated below.
- Close the browser to close the report.

DC IR Drop Simulation Report

SIwave Version: 2015.0.0
Creation Date: Fri Jan 09 11:39:11 2015

Design File: DCIR.siw
Simulation Name: DC IR Sim 1

Layer Stack-up

| Name | Type | Thickness(mm) | Material | Conductivity(S/m) | Dielectric Constant | Loss Tangent | Transverse | Elevation(mm) | Roughness(mm) | Current Plot | Voltage Plot | Power Plot |
|-------------|------------|---------------|------------|-------------------|---------------------|--------------|------------|---------------|---------------|-------------------------------------|-------------------------------------|-------------------------------------|
| UNNAMED_000 | DIELECTRIC | 0 | EDB_AIR | 0 | 1 | 0 | | 2.03454 | | | | |
| TOP | METAL | 0.04826 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 1.98628 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_002 | DIELECTRIC | 0.06711 | EDB_FR-4_3 | 0 | 3.56 | 0.024 | 80 | 0.91897 | | | | |
| PWR | METAL | 0.03302 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 1.98595 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_004 | DIELECTRIC | 0.27 | EDB_FR-4_2 | 0 | 4.34 | 0.018 | | 0.61595 | | | | |
| LYR_1 | METAL | 0.03048 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 0.38547 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_006 | DIELECTRIC | 0.2032 | EDB_FR-4_1 | 0 | 4.5 | 0.035 | | 0.38227 | | | | |
| LYR_2 | METAL | 0.03048 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 0.35179 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_008 | DIELECTRIC | 0.2032 | EDB_FR-4_1 | 0 | 4.5 | 0.035 | | 0.14839 | | | | |
| GND | METAL | 0.03302 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 0.11557 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_010 | DIELECTRIC | 0.06711 | EDB_FR-4 | 0 | 3.56 | 0.024 | | 0.04826 | | | | |
| BOTTOM | METAL | 0.04826 | EDB_COPPER | 5.959E+07 | 1 | 0 | 80 | 0 | HJ: 0, HJ: 0 | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| UNNAMED_012 | DIELECTRIC | 0 | EDB_AIR | 0 | 1 | 0 | | 0 | | | | |

Current Plot Voltage Plot Power Plot
VIA ☒ ☒ ☒

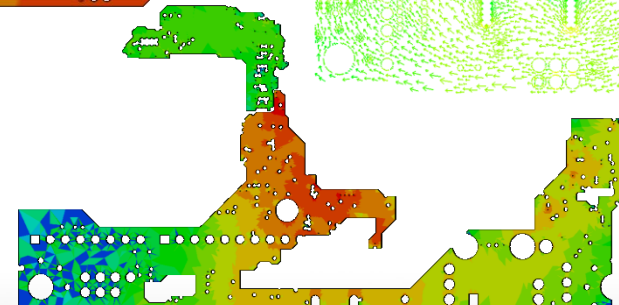
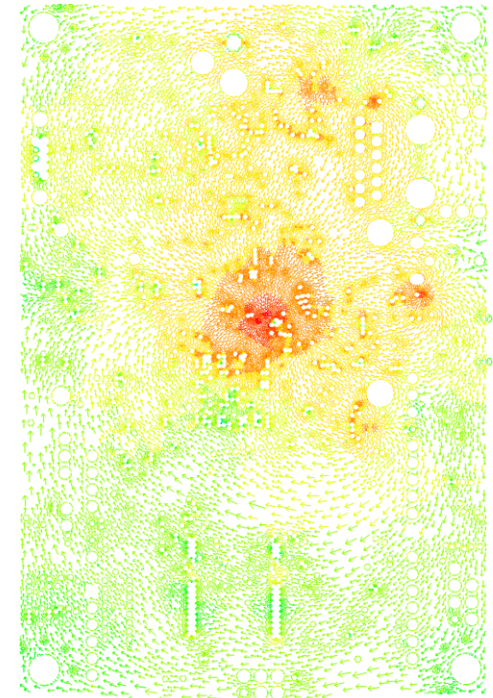
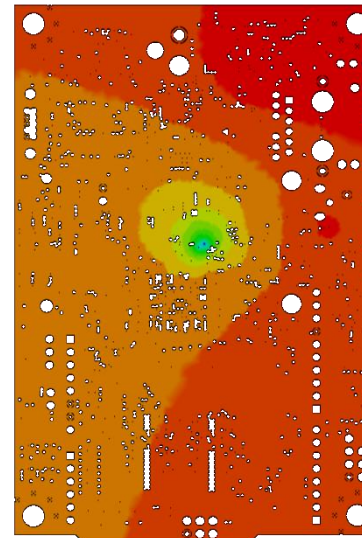
Plots grouped by: Layer (Switch to group by Plot Type)

Current Sources

| Name | Magnitude(A) | Phase(degrees) | Source Resistance(ohms) | Positive Terminal | Negative Terminal | Positive Terminal | Negative Terminal | Simulation Results |
|------------------------------------|--------------|----------------|-------------------------|-------------------|-------------------|--|--------------------------------------|---------------------------------------|
| U2A5_AA26_V3P3_S0 | 0.333333 | 0 | 5E+07 | V3P3_S0 | GND | AA26(U2A5) | GND_IPD031-201_U2A5_DCFLOWSink(U2A5) | 8.582726499426e+08 3.291363249713e+00 |
| U2A5_AB24_V3P3_S0 | 0.333333 | 0 | 5E+07 | V3P3_S0 | GND | AB24(U2A5) | GND_IPD031-201_U2A5_DCFLOWSink(U2A5) | 8.582840386208e+08 3.291420193104e+00 |
| U2A5_AD24_V3P3_S0 | 0.333333 | 0 | 5E+07 | V3P3_S0 | GND | AD24(U2A5) | GND_IPD031-201_U2A5_DCFLOWSink(U2A5) | 8.582883656930e+08 3.291441828465e+00 |
| V3P3_S0_C76254-001_U3B2_DCFLOWSink | 0.3 | 0 | 5E+07 | V3P3_S0 | GND | V3P3_S0_C76254-001_U3B2_DCFLOWSink(U3B2) | GND_C76254-001_U3B2_DCFLOWSink(U3B2) | 8.583651640163e+08 3.292825820082e+00 |
| V3P3_S0_G60296-001_U4B1_DCFLOWSink | 0.5 | 0 | 5E+07 | V3P3_S0 | GND | V3P3_S0_G60296-001_U4B1_DCFLOWSink(U4B1) | GND_G60296-001_U4B1_DCFLOWSink(U4B1) | 8.583706950029e+08 3.291853475015e+00 |
| V3P3_S0_G83474-001_U2B1_DCFLOWSink | 0.2 | 0 | 5E+07 | V3P3_S0 | GND | V3P3_S0_G83474-001_U2B1_DCFLOWSink(U2B1) | GND_G83474-001_U2B1_DCFLOWSink(U2B1) | 8.586185712165e+08 3.293097856083e+00 |

Voltage Sources

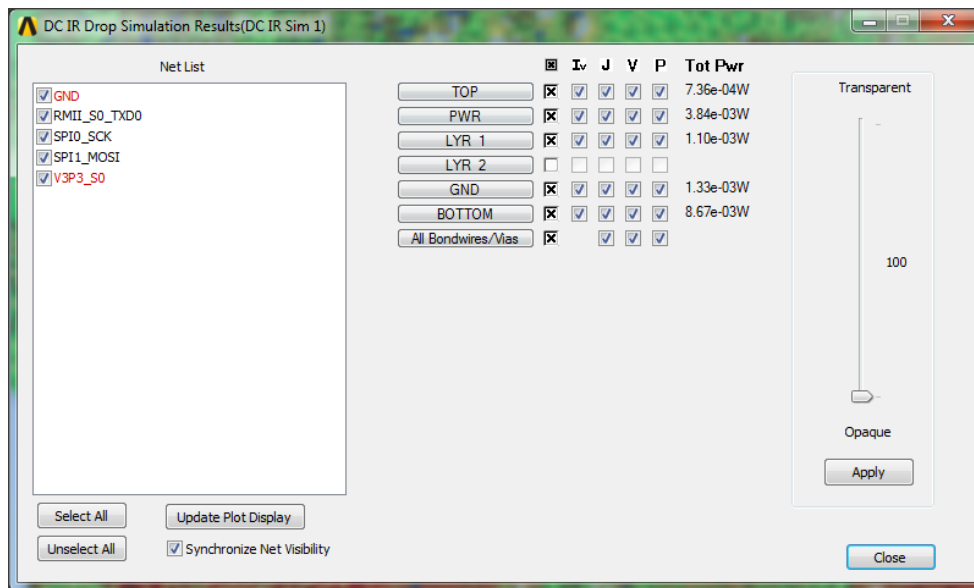
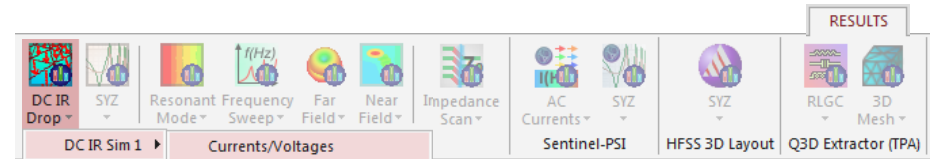
| Name | Magnitude(V) | Phase(degrees) | Source Resistance(ohms) | Positive Terminal | Negative Terminal | Positive Terminal | Negative Terminal | Simulation Results |
|-----------------------------------|--------------|----------------|-------------------------|-------------------|-------------------|---|-------------------------------------|---------------------------------------|
| V3P3_S0_G94441-001_U2M1_DCFLOWVRM | 3.3 | 0 | 1E+06 | V3P3_S0 | GND | V3P3_S0_G94441-001_U2M1_DCFLOWVRM(U2M1) | GND_G94441-001_U2M1_DCFLOWVRM(U2M1) | 2.000358665377e+00 0.000358665377e+00 |



DC Simulation Results

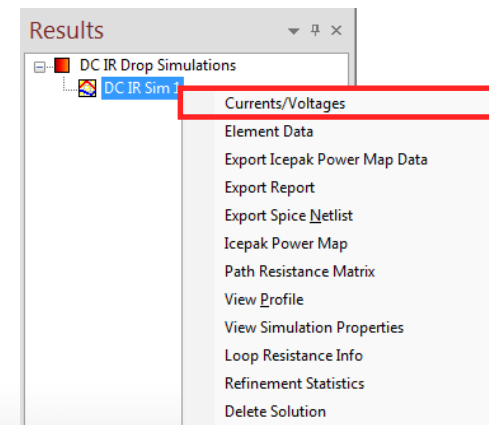
• Results

- From the Results menu, choose:
 - **DC IR Drop > DC IR Sim 1 > Currents/Voltages**
- This will open the DC Results plotting window.



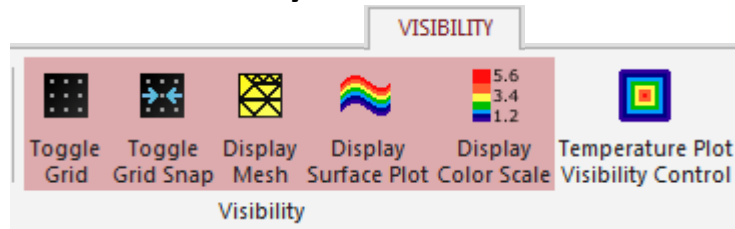
- Element Data
- Export Icepak Power Map Data
- Export Report
- Export Spice Netlist
- Icepak Power Map
- Path Resistance Matrix
- View Profile
- View Simulation Properties
- Loop Resistance Info
- Refinement Statistics
- Delete Solution

- Alternatively, from the results window:
 - **Double-click DC IR Sim 1**
 - or
 - **Right-click DC IR Sim 1 > Currents/Voltages**

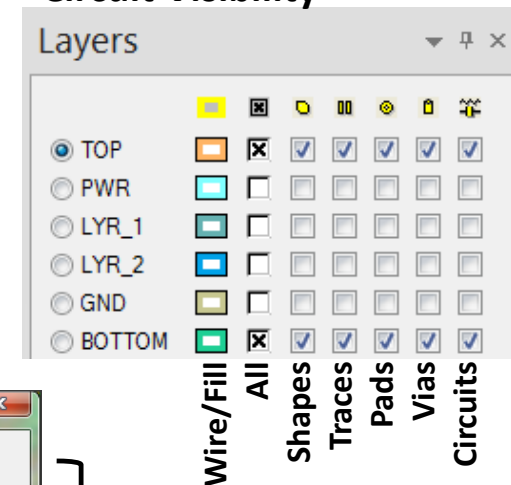


DC Simulation Results: Display

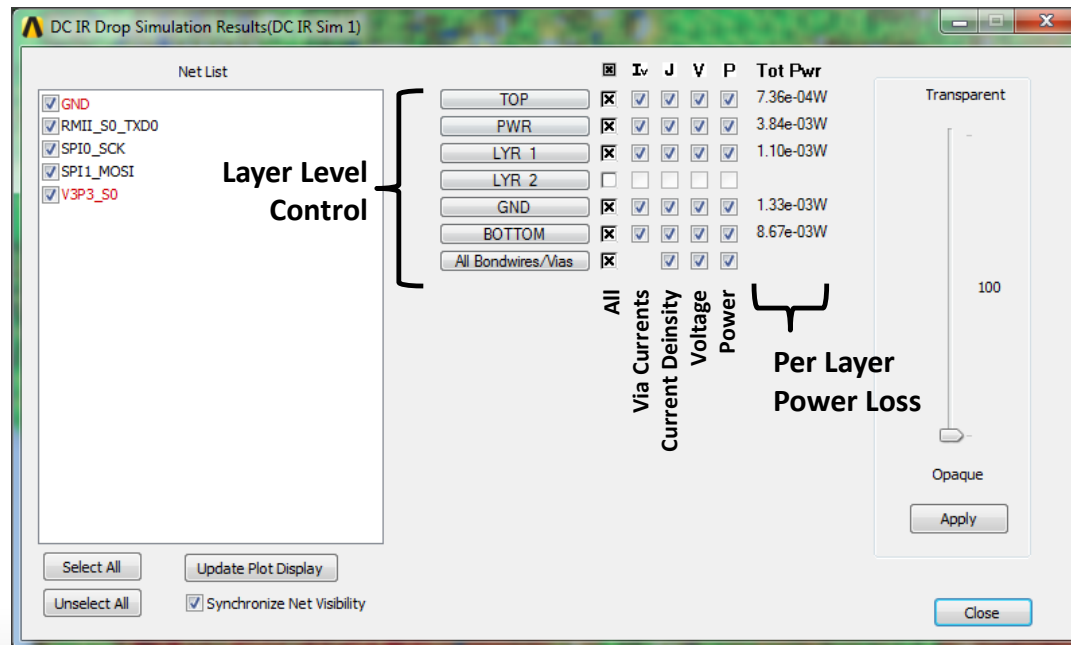
Global Visibility



Geometry and Circuit Visibility



Individual Plot Visibility



Net Level Control

Layer Level Control

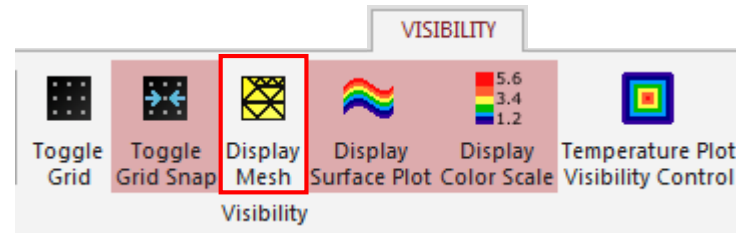
Per Layer Power Loss

Opacity

DC Simulation Results: Display

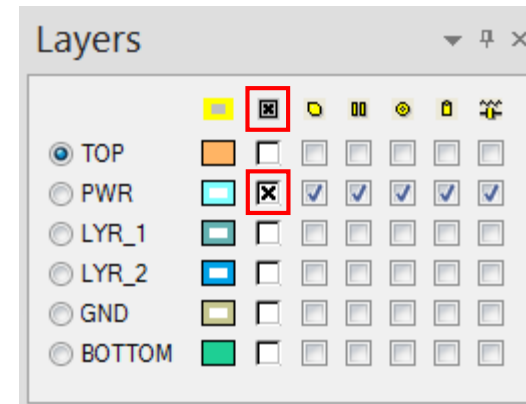
- **Disable Mesh Display**

- Click the Display Mesh button to an untoggled state.



- **Enable visibility of the PWR Layer**

- **Disable visibility** of all layers by clicking on the column header icon.
- **Enable visibility** of all objects on the PWR layer by clicking in the indicated toggle all box.
- Note: Geometry visibility is not necessary for plot display.



DC Simulation Results: Plotting

- **DC IR Drop on the PWR Layer**

- Net Level Control

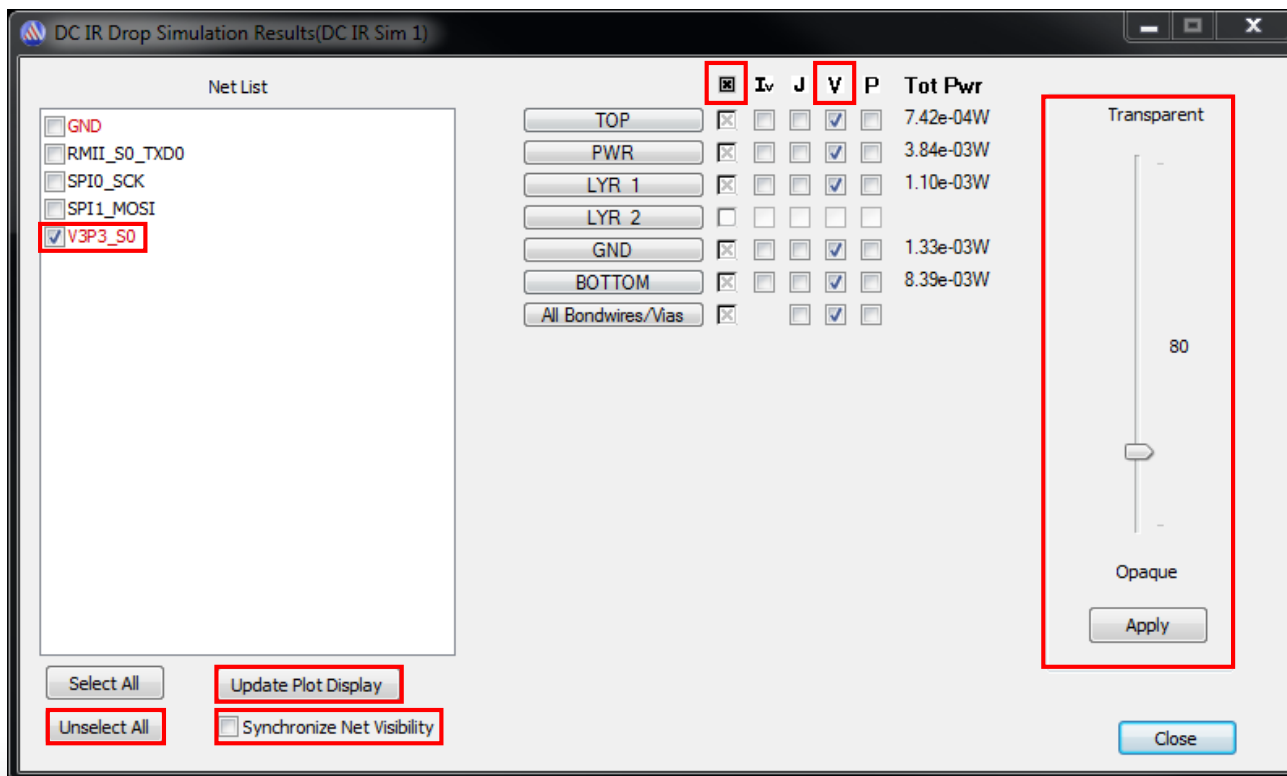
- Click the **Unselect All** button to uncheck all nets.
- Click the **check box** next to **V3P3_S0** to enable the net.
- Uncheck **Synchronize Net Visibility**.
- Click **Update Plot Display**.

- Layer Level Control

- Click the **Toggle All** column header icon to uncheck all plots.
- Click the indicated **Voltage** plot for the **PWR** layer.

- Opacity

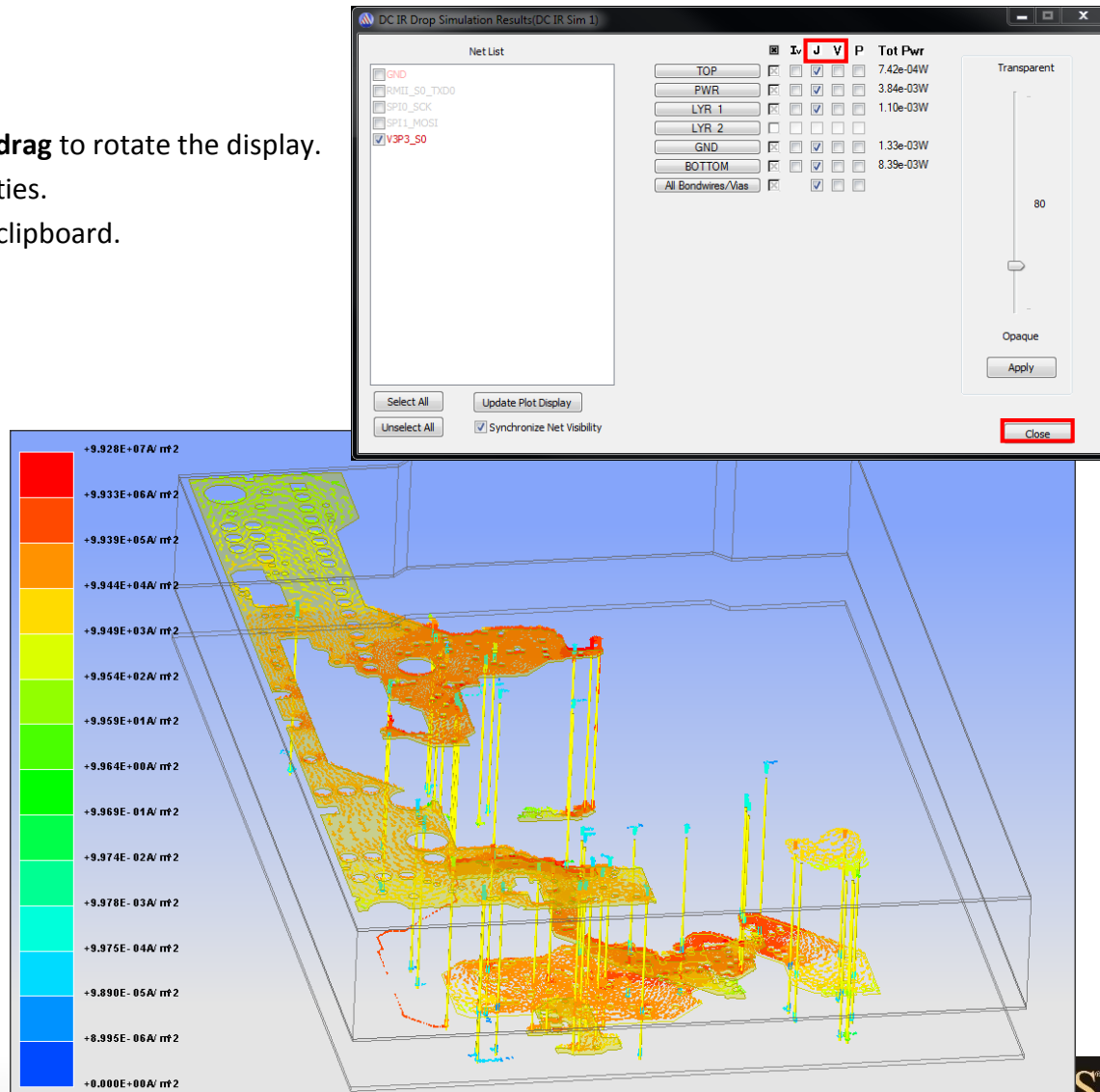
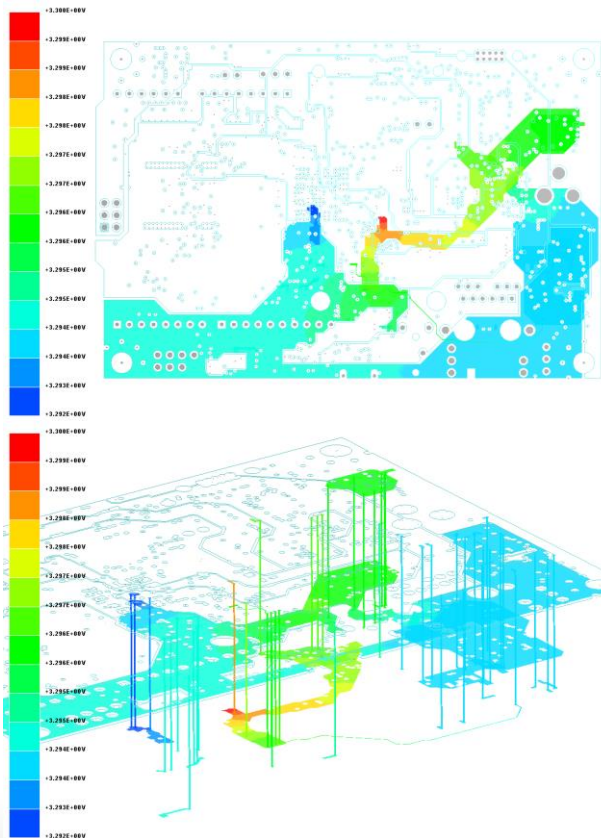
- Move the slider bar to **80**.
- Click **Apply**.



DC Simulation Results: Plotting

- **Plotting Results**

- Your plot should look as shown below.
- Hold the **Alt** key and use the mouse to **click and drag** to rotate the display.
- Change the plot settings to view different quantities.
- **Right-click > Copy Image** to send the plot to the clipboard.




DC Simulation Results: High Current Vias

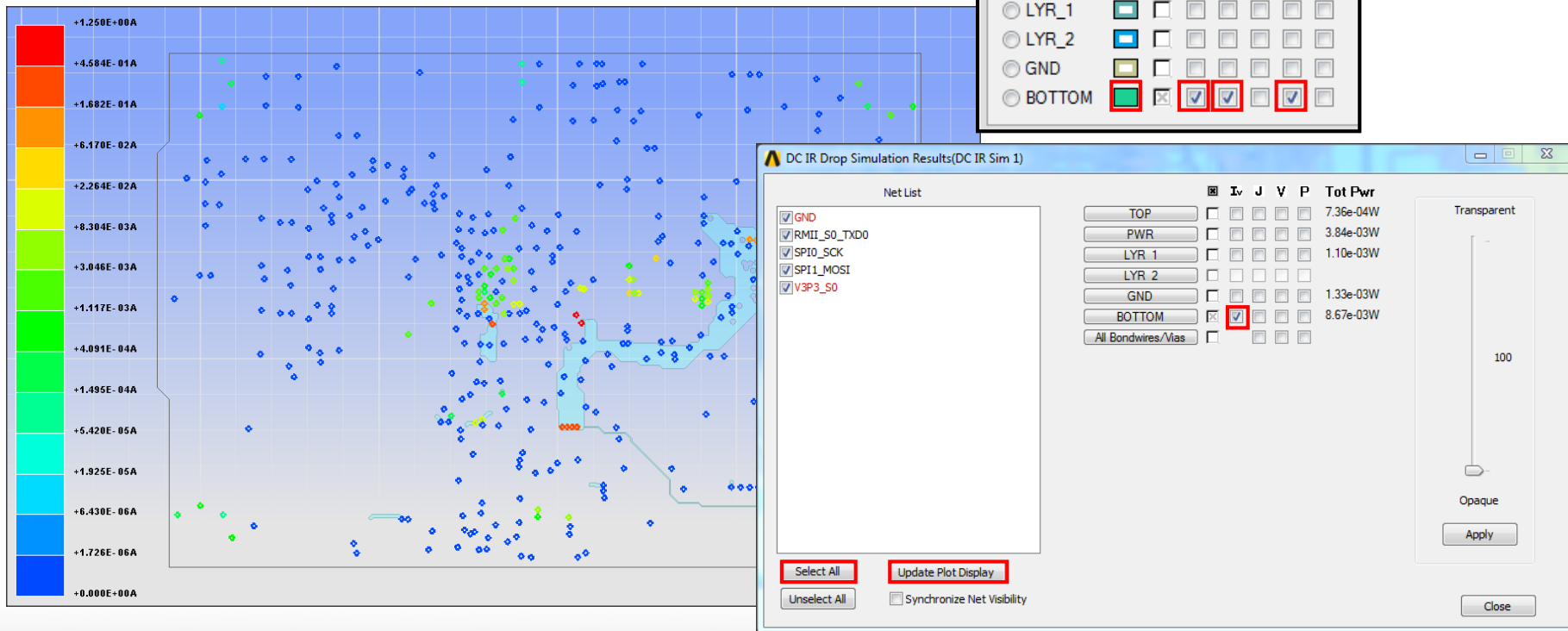
- **Identifying High Current Vias**

- In the DC Simulation Results window:

- Click **Select All**
- Click **Update Plot Display**
- Check only the **I_v** box for layer **BOTTOM**

- In the Layers window:

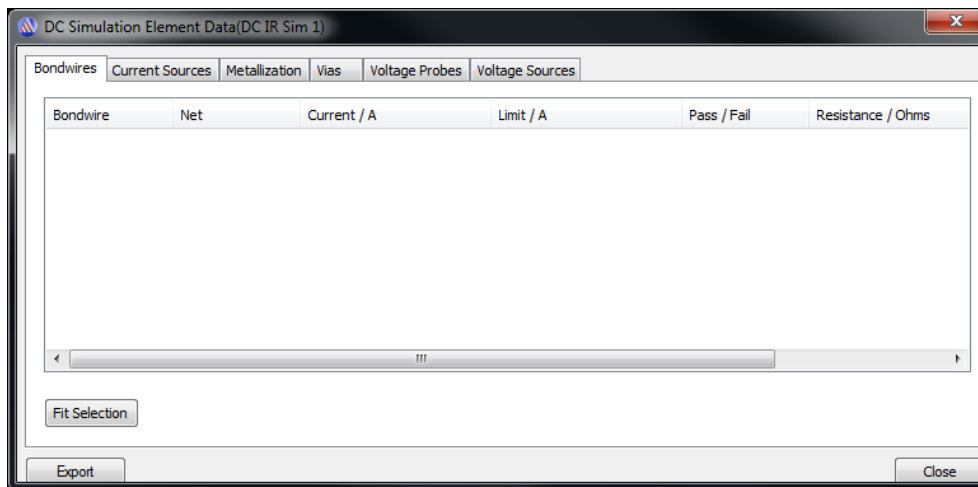
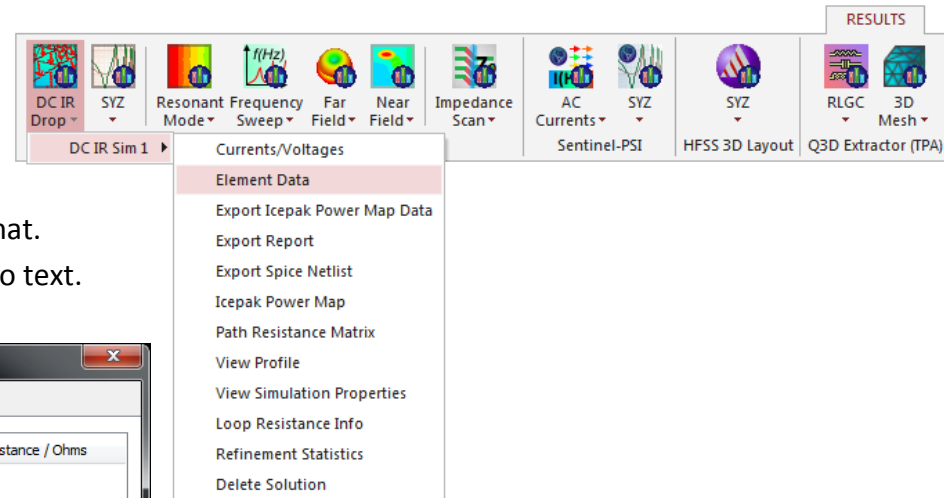
- Uncheck all boxes by clicking on the  on.
- Check the boxes for **Fill**, **Shape**, **Trace**, and **Via** as shown.



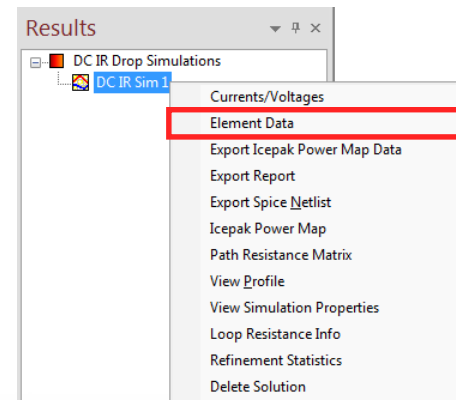
DC Simulation Results: High Current Vias

- **Element Data**

- From the Results menu, choose:
 - **DC IR Drop > DC IR Sim 1 > Element Data**
- This will open the Element Data Window.
 - Element Data has access to all calculated data in a raw format.
 - Use it to fit specific quantities in the GUI or to export data to text.



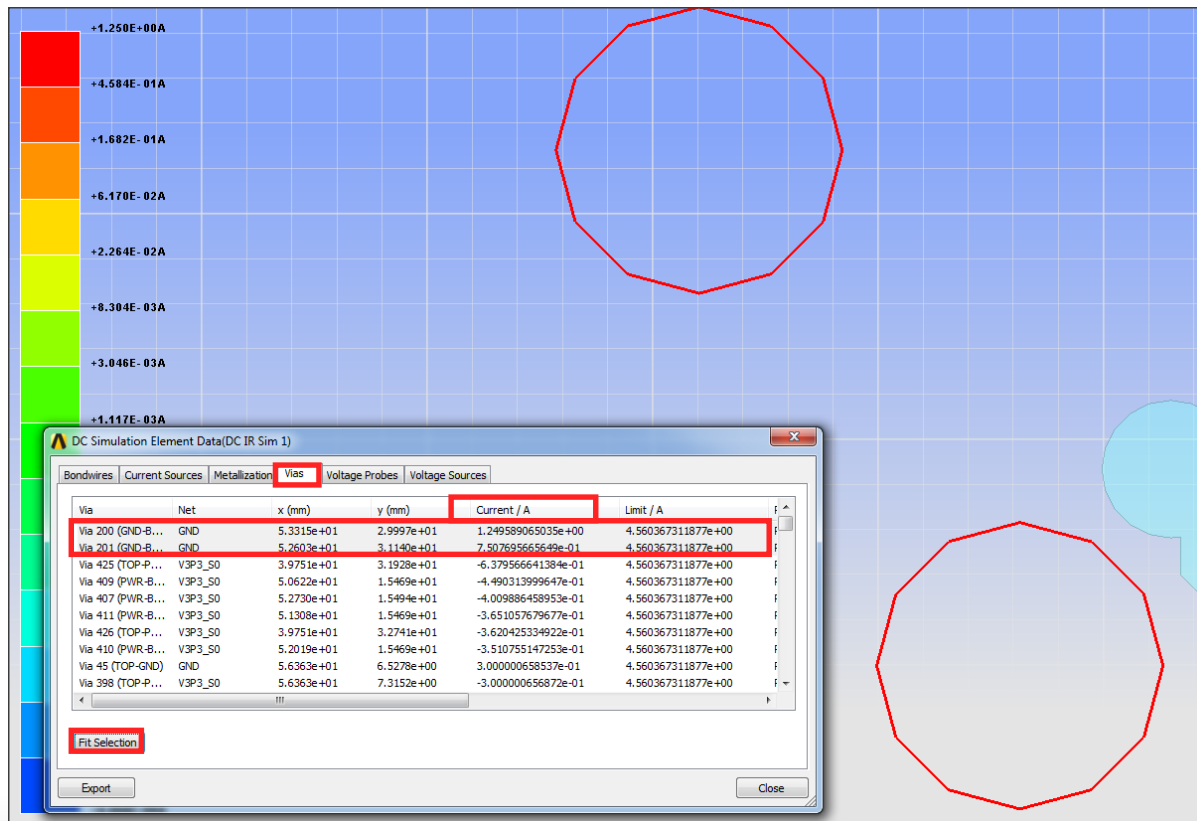
- Alternatively, from the results window:
 - **Right-click DC IR Sim 1 > Element Data**



DC Simulation Results: High Current Vias

- **Identifying High Current Vias**

- Click the **Vias** tab in the Element Data window.
- Click the **Current / A** column header to sort by column.
- Select the top two rows using **shift+click** or **ctrl+click**. This represents the two vias with the highest current.
- Click the **Fit Selection** button.
 - The display will zoom into this location and highlight the vias in yellow.
- Click **Close**.

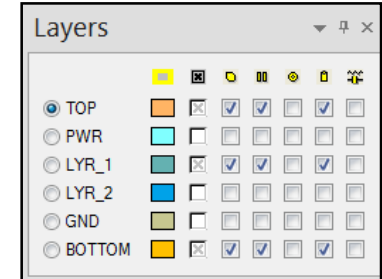


DC Simulation Results: High Current Vias

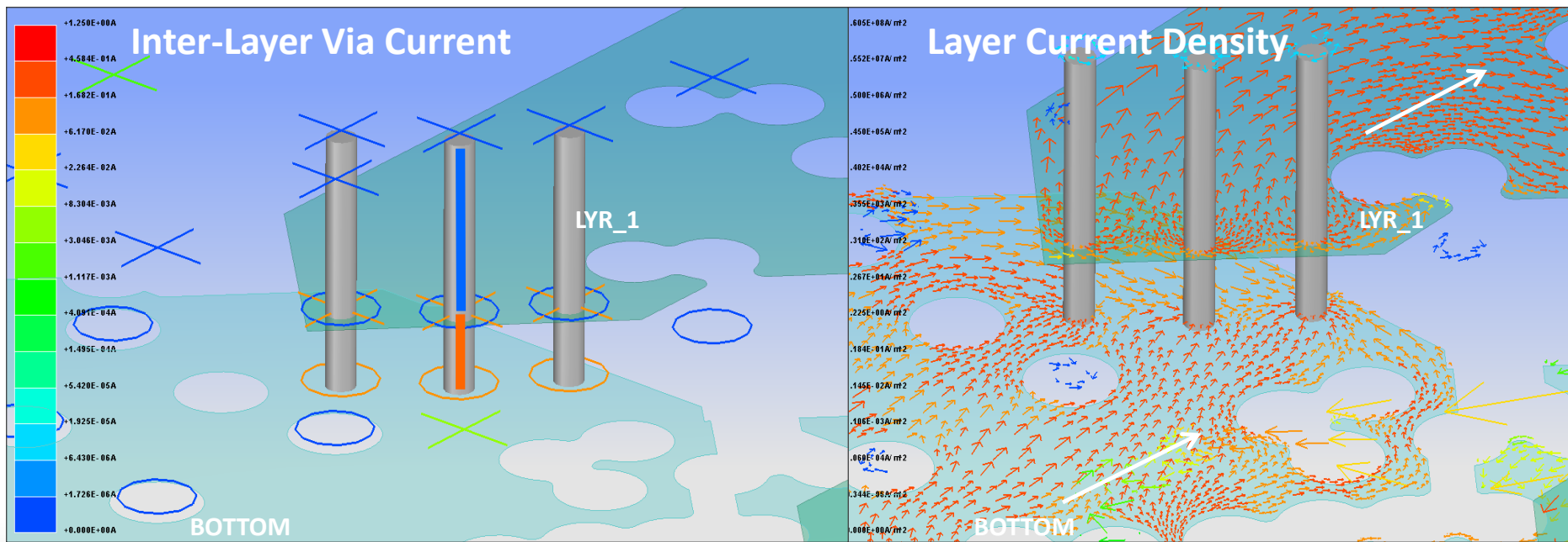
- **Explanation of Via Currents, I_v**

- O and X represent current magnitude between layers.
 - O is current to a layer towards the top of the stackup.
 - X is current to a layer away from the top of the stackup.

| | I_v | J | V | P | Tot Pwr |
|--------------------|-------------------------------------|-------------------------------------|--------------------------|--------------------------|-----------|
| TOP | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | 7.36e-04W |
| PWR | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | 3.84e-03W |
| LYR_1 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | 1.10e-03W |
| LYR_2 | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | |
| GND | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | 1.33e-03W |
| BOTTOM | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | 8.67e-03W |
| All Bondwires/Vias | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | <input type="checkbox"/> | |

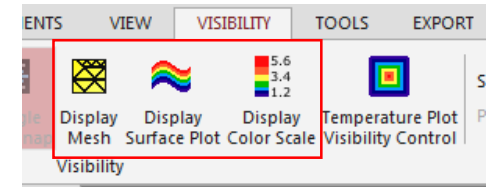


- In this example, current is carried from layer BOTTOM to LYR_1 through three vias. The **red O** and **X** represent a magnitude of current going between these two layers.
- The current does not continue to travel up to the TOP layer. This is indicated by the **blue O** and **X** on LYR_1 and TOP, respectively.
- Note that Via current is magnitude only (A) whereas Layer Current Density displays vectors (A/m²).

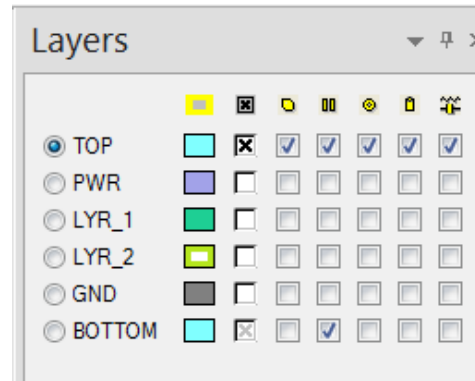


DC Path Resistance

- Under the *Visibility* menu disable the *Surface plot* and the *Colour Scale*

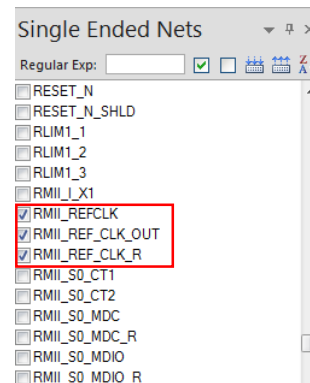


- Set up the Layers visibility as illustrated



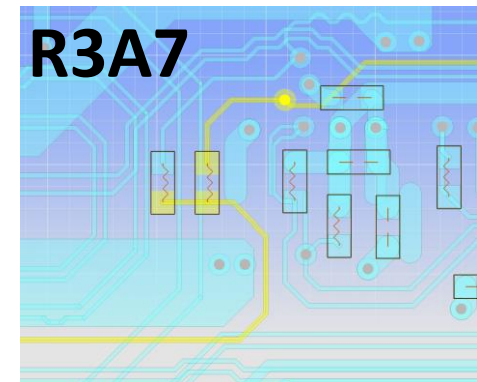
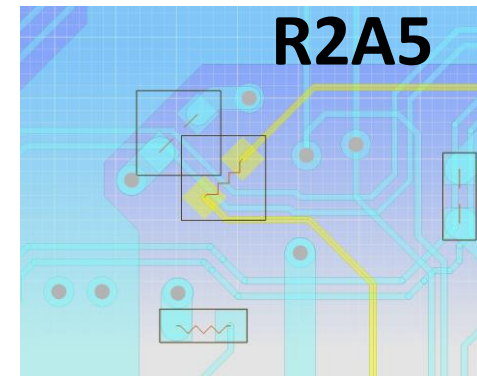
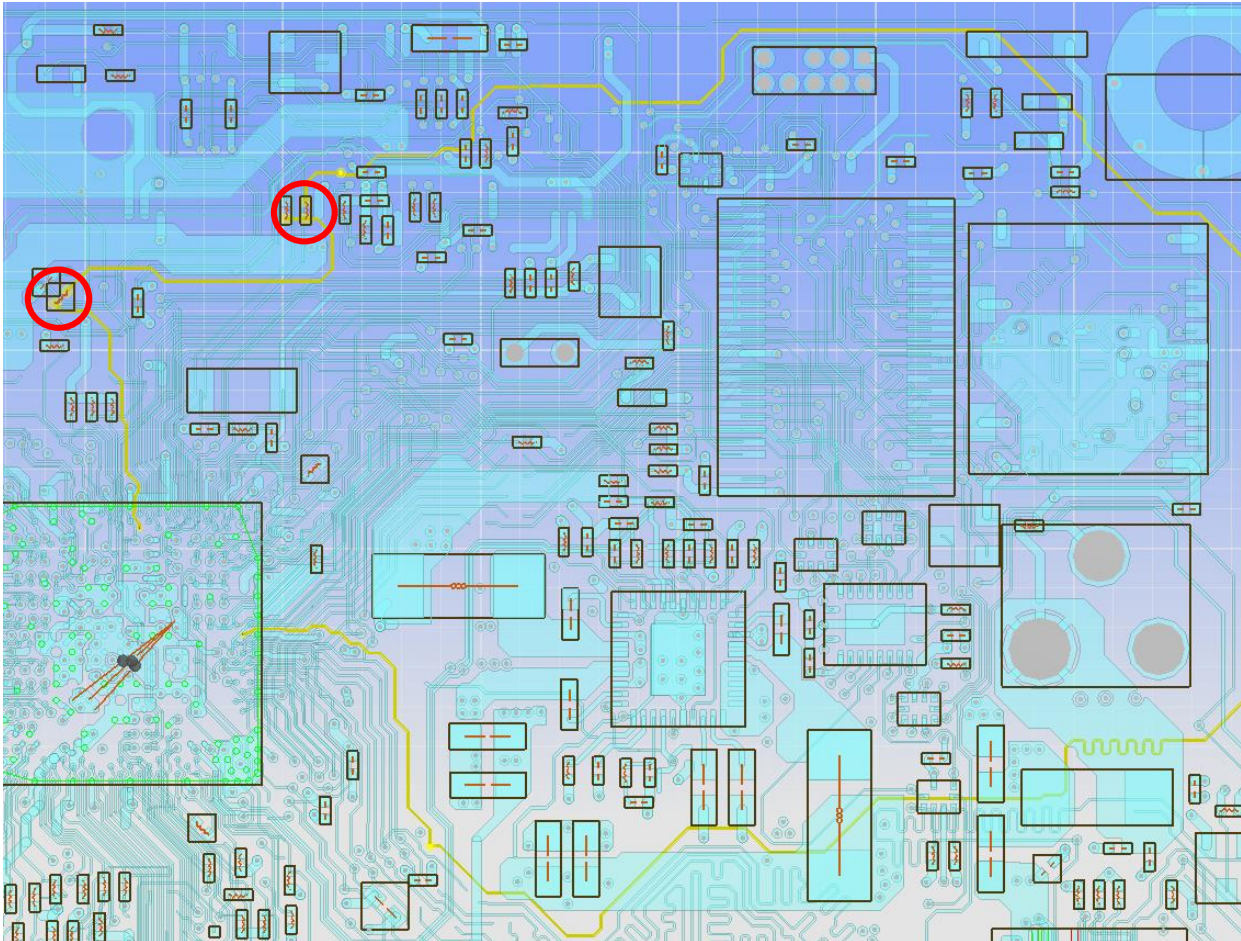
- Right click on the nets list and choose:

- RMII_REFCLK
- RMII_REF_CLK_OUT
- RMII_REF_CLK_R



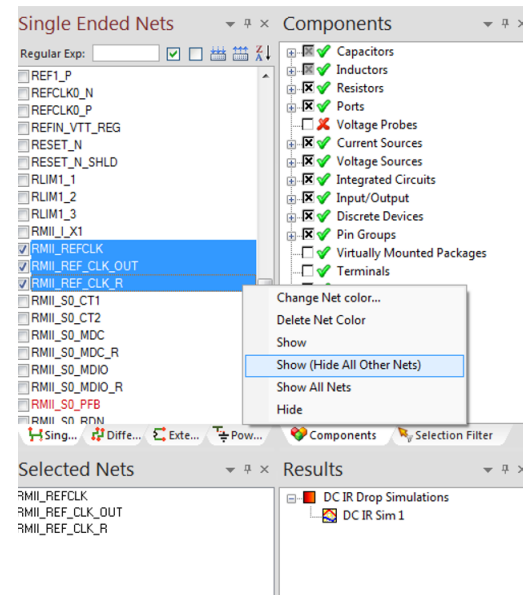
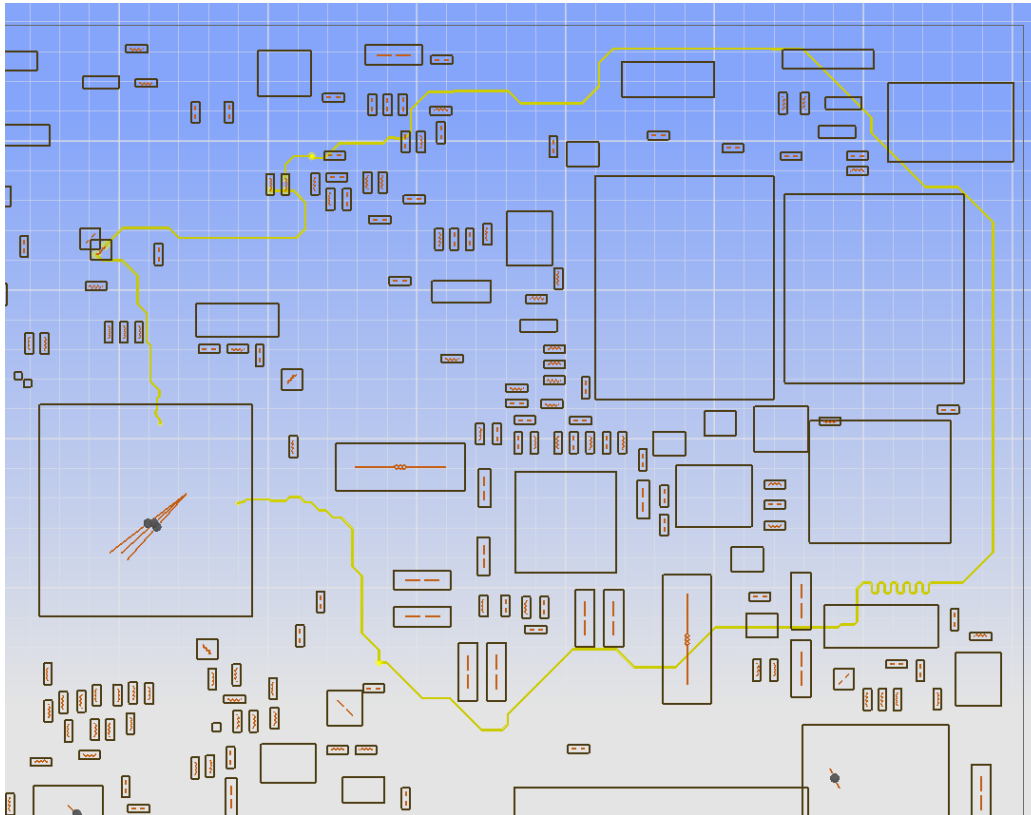
DC path resistance

- The settings highlights in yellow a full net that runs across top and bottom layers, including vias and components such as resistors called: R2A5 and R3A7



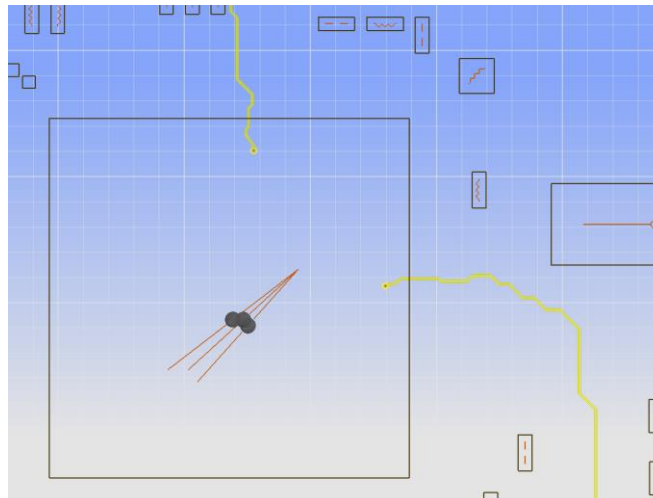
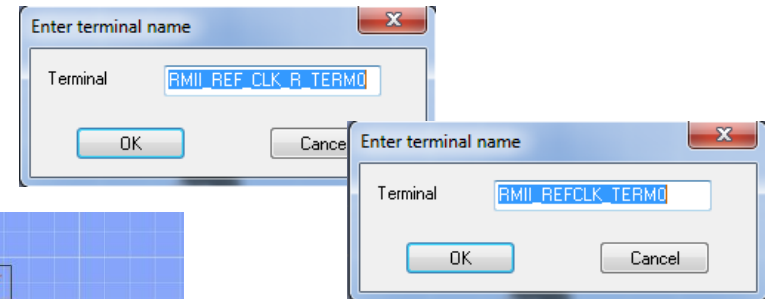
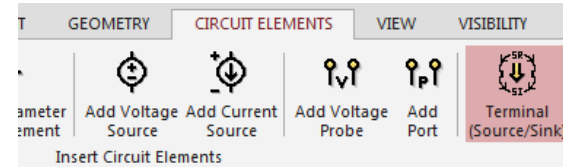
DC Path Resistance

- Highlights the three nets using CTRL button
- Right Click and choose *Show(Hide All Other Nets)*



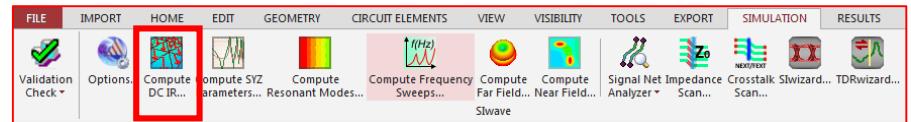
DC Path Resistance

- Under the Circuit Elements menu, select the *Terminal(Source/Sink)* tool
- Then Insert the terminals with left mouse click at the start and end points on the nets. (They happen to be under the same IC area)
- A pop up window will ask to confirm the net on which the terminal is attached.
- Click OK for both ends.

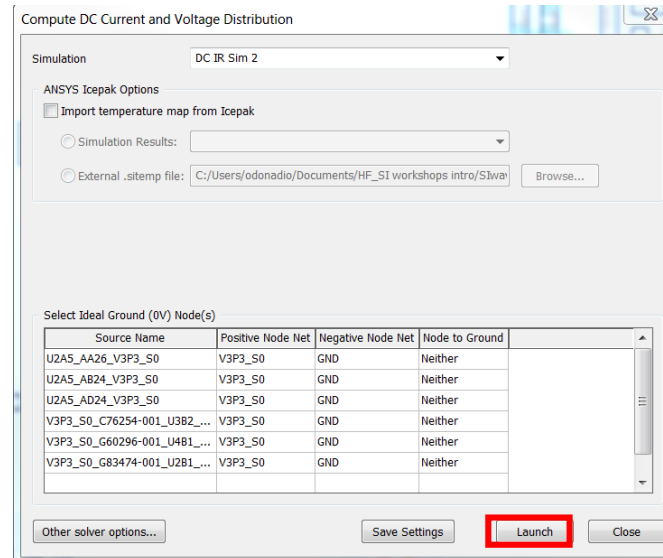


DC Path Resistance

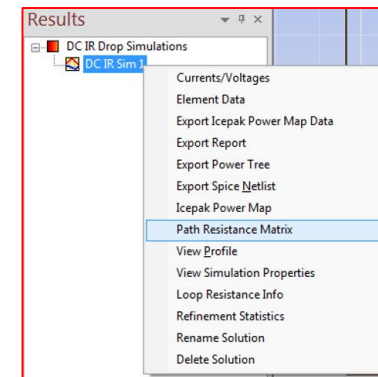
- Under Simulation tab select the icon to *Compute DC IR drop*



- Click *Launch* then *Yes*



- When the simulation ends, right click on the results
- Choose *Path Resistance Matrix* from the drop down menu



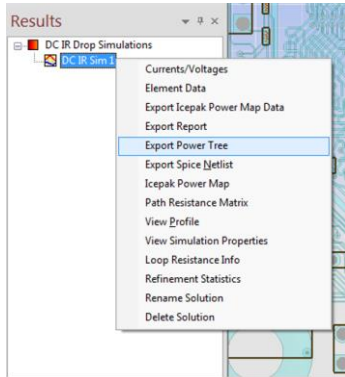
DC Path Resistance

- The Resistance Path Matrix shows **33.21 Ohms** calculated between the two terminals.
- This is consistent with the series resistor values
 - R2A5=10 Ohms
 - R3A7=22.6 Ohms

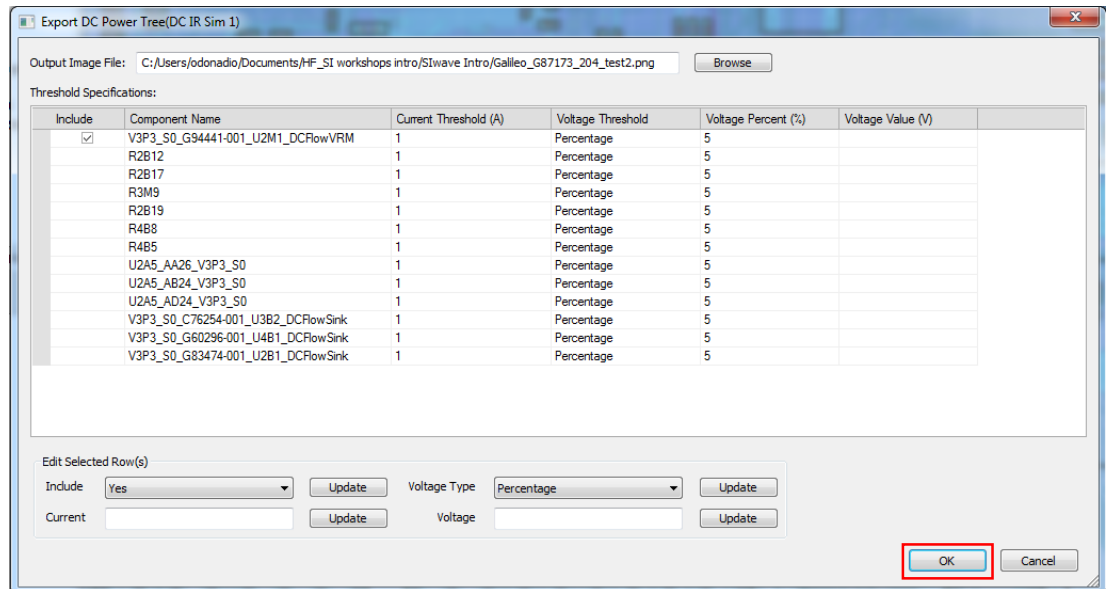
| | RMII_REFCLK_TERM0 | RMII_REF_CLK_R_TERM0 | U2A5_AA26_V3P3_S0_n | U2A5_AA26_V3P3_S0_p | U2A5_AB |
|--------------------------------------|-------------------|----------------------|---------------------|---------------------|-----------|
| RMII_REFCLK_TERM0 | | 3.319722e+01 | Inf | Inf | Inf |
| RMII_REF_CLK_R_TERM0 | 3.319722e+01 | | Inf | Inf | Inf |
| U2A5_AA26_V3P3_S0_n | Inf | Inf | | 9.166691e+03 | 0.000000e |
| U2A5_AA26_V3P3_S0_p | Inf | Inf | 9.166691e+03 | | 9.166691e |
| U2A5_AB24_V3P3_S0_n | Inf | Inf | 0.000000e+00 | 9.166691e+03 | |
| U2A5_AB24_V3P3_S0_p | Inf | Inf | 9.166691e+03 | 3.825512e-04 | 9.166691e |
| U2A5_AD24_V3P3_S0_n | Inf | Inf | 0.000000e+00 | 9.166691e+03 | 0.000000e |
| U2A5_AD24_V3P3_S0_p | Inf | Inf | 9.166691e+03 | 6.022108e-04 | 9.166691e |
| V3P3_S0_C76254-001_U3B2_DCFlowSink_n | Inf | Inf | 2.734176e-03 | 9.166693e+03 | 2.734176e |
| V3P3_S0_C76254-001_U3B2_DCFlowSink_p | Inf | Inf | 9.166694e+03 | 7.127299e-03 | 9.166694e |
| V3P3_S0_G60296-001_U4B1_DCFlowSink_n | Inf | Inf | 1.244745e-03 | 9.166692e+03 | 1.244745e |
| V3P3_S0_G60296-001_U4B1_DCFlowSink_p | Inf | Inf | 9.166695e+03 | 9.104505e-03 | 9.166695e |
| V3P3_S0_G83474-001_U2B1_DCFlowSink_n | Inf | Inf | 8.508499e-04 | 9.166691e+03 | 8.508499e |
| V3P3_S0_G83474-001_U2B1_DCFlowSink_p | Inf | Inf | 9.166689e+03 | 2.786657e-03 | 9.166689e |
| V3P3_S0_G94441-001_U2M1_DCFlowVRM_n | Inf | Inf | 6.862551e-04 | 9.166691e+03 | 6.862551e |
| V3P3_S0_G94441-001_U2M1_DCFlowVRM_p | Inf | Inf | 9.166692e+03 | 5.412539e-03 | 9.166692e |

DC Power Tree

- Right Click on the results and choose *Export Power Tree*

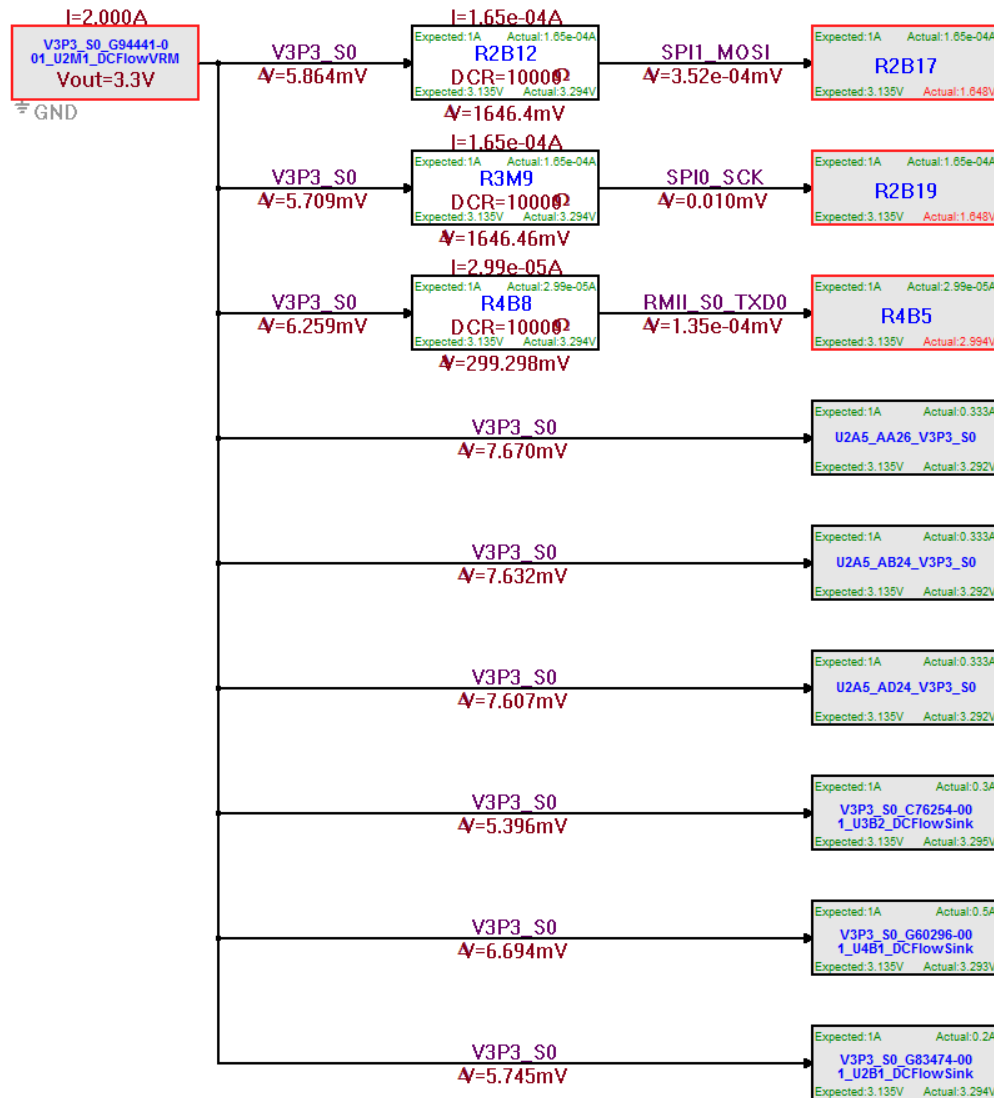


- Click OK



- This will export a Signal Flow Graph in the same directory of the SIwave project.

DC Power Tree

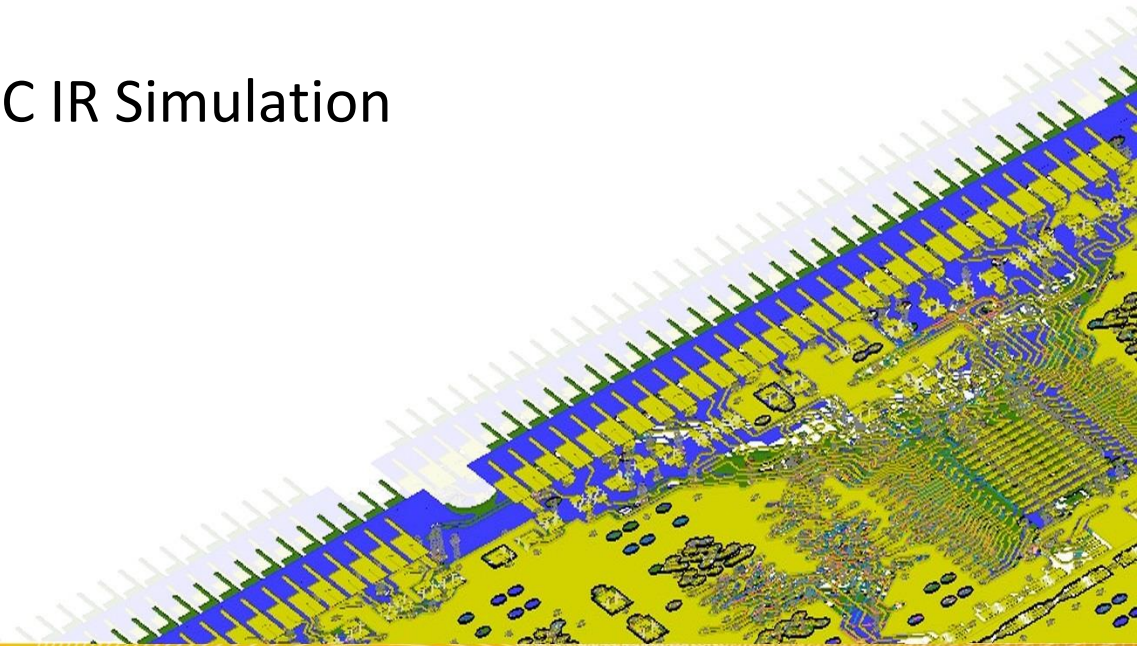


| Actual Voltage | Actual Current | IR Drop | Specification | Pass/Fai |
|----------------|----------------|--------------------|---------------|----------|
| 1.648V | 1.65e-04A | Δ=1652.27mV(50.1%) | 3.3V(+/-5.0%) | Fail_V |
| 1.648V | 1.65e-04A | Δ=1652.18mV(50.1%) | 3.3V(+/-5.0%) | Fail_V |
| 2.994V | 2.99e-05A | Δ=305.557mV(9.3%) | 3.3V(+/-5.0%) | Fail_V |
| 3.292V | 0.333A | Δ=7.670mV(0.2%) | 3.3V(+/-5.0%) | Pass |
| 3.292V | 0.333A | Δ=7.632mV(0.2%) | 3.3V(+/-5.0%) | Pass |
| 3.292V | 0.333A | Δ=7.607mV(0.2%) | 3.3V(+/-5.0%) | Pass |
| 3.295V | 0.3A | Δ=5.396mV(0.2%) | 3.3V(+/-5.0%) | Pass |
| 3.293V | 0.5A | Δ=6.694mV(0.2%) | 3.3V(+/-5.0%) | Pass |
| 3.294V | 0.2A | Δ=5.745mV(0.2%) | 3.3V(+/-5.0%) | Pass |



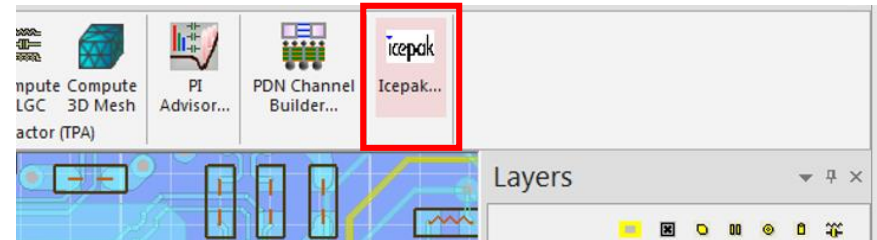
Thermal Analysis (Optional)

DC IR Simulation

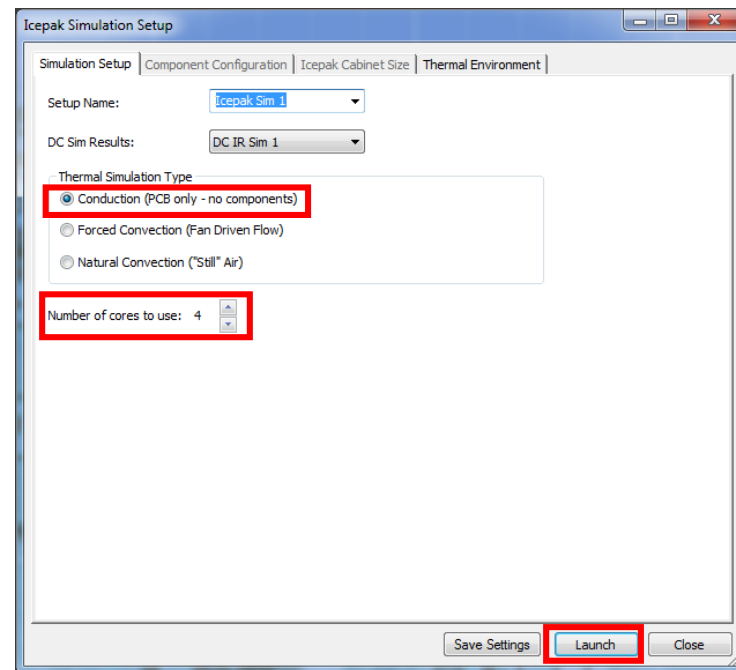


Thermal Analysis: Icepak integration

- From the Simulation tab select the Icepak button



- Select the *Conduction* radio button to simulate the thermal gradient on the PCB board
- Set the number of cores to use to 4
- Then *Launch* the simulation



Thermal Analysis: Icepak integration

- At the end of the simulation the Results window will be populated with the results from Icepak
- Right Click on *Icepak Sim 1* and choose *Display Temperature* to inspect the temperature map/distribution on the PCB due to the current/voltage sources set at the beginning of the workshop

