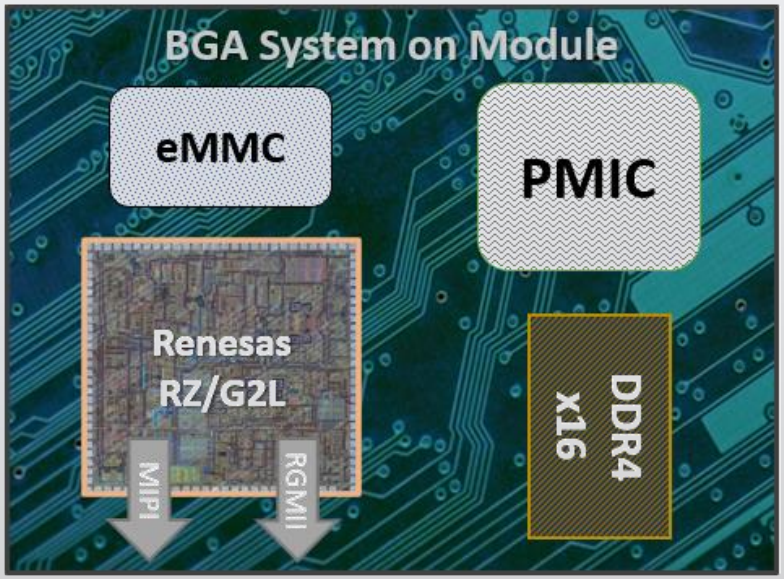
TIEplus 2023 - Subject Overview

- The diagram below describes the simplified architecture of a System-on-Module PCB that is based on an ARM-Cortex SoC



- Your task is to ensure the signal integrity of the DDR4 interface considering also the influence of the power delivery network

- Required skills: s-parameter (touchstone file) analysis and processing; timing analysis; full-wave solver extraction; transient simulation; IO modeling; crosstalk analysis; eye-diagram analysis; power-aware IBIS modeling; SI-PI co-simulation

TIEplus 2023 - Requirements

- Requirements:

  A. Analyze power integrity for DC and AC domains for 1V2_DDR power rail. Select decoupling capacitors in order to meet target impedance for both SoC and DRAM.
  * Use capacitor models from Murata MLCC lineup (www.murata.com) series GRM - SimSurfing tool
  * Capacitor case size is restricted to layout design (package size also mention on schematic)
  * Capacitors C133-C138 fixed part number: GRM188R60J476ME15
  * Capacitors C35-C41 ,C43-C46, C50-C56, C63-C69 part number: must be selected based on PDN design

  B. Evaluate DDR4 interface routing based on the following criteria: impedance, timing skew, crosstalk. Define corrective actions for the layout team if necessary.
  * Actual layout design modifications are not required, only the description of corrective actions.

  C. Perform full channel transient simulation for all DDR signal lines. Evaluate eye diagram performance at the receiver. Find optimal drive strength and ODT settings.

  D. Include the effects of VDDQ PDN into the channel transient simulation by using the power-aware capabilities of the provided DRAM IBIS model. Re-evaluate eye diagram margins considering SI-PI co-simulation.

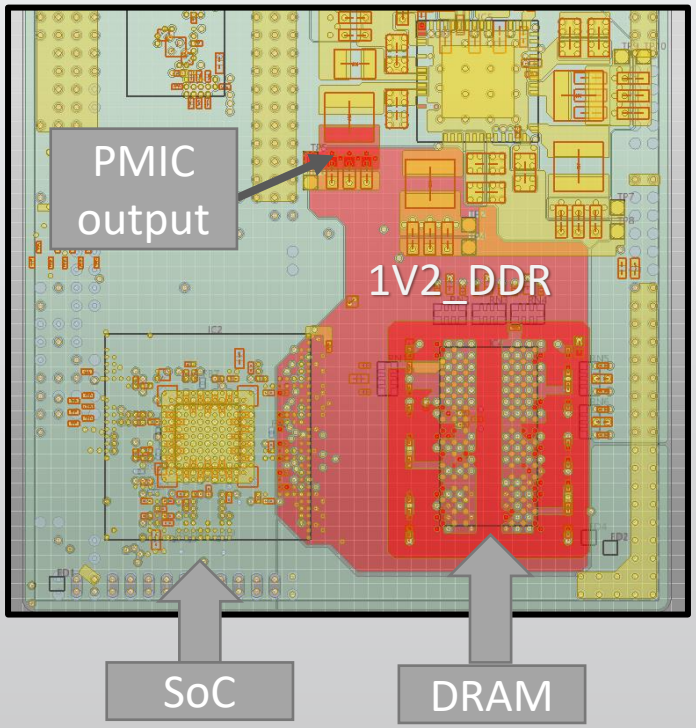
- Operating conditions:
  - Data rate: 1600MT/s
  - IC temperature range: industrial, Tc: -40..95°C, Tj: -40..125°C

Notes:
- Transient simulation must be performed across all IBIS PVT corners.
- Channel = complete interconnect path from driver to receiver.

TIEplus 2023

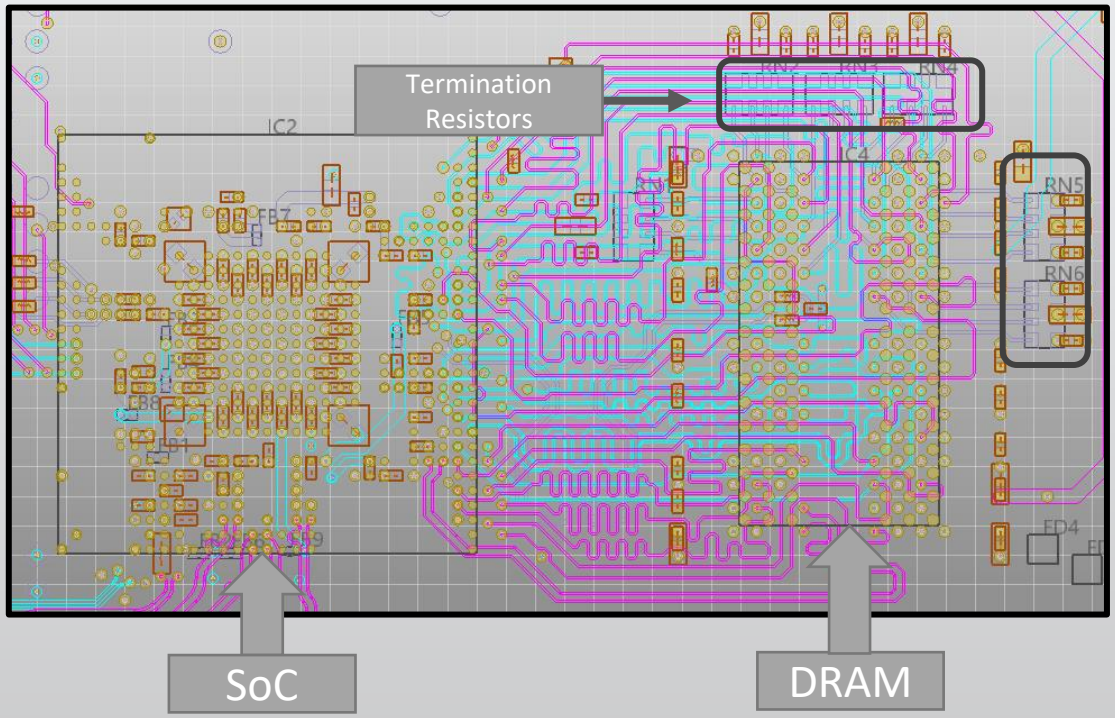
Detailed Diagram

1V2 Power Delivery



Distribution of 1V2_DDR plane is done mainly on L5 with local power islands on TOP and BOT.
Decupling capacitors for DRAM are placed on TOP side.
Decupling capacitors for SoC are placed on BOT side.
*Decoupling capacitors type and values are not defined.
*Footprint selection is restricted to layout implementation.

Signal Routing



The routing of DDR interface signals is done on L3 and L8, in stripline configuration. The terminations for the command and address signals are implemented using resistor networks.

TIEplus 2023
Input Data Summary

Item	Location	Description
PCB data	TIEplus23_SOM_pcb.zip (ODB++) TIEplus23_SOM_pcb.edb TIEplus23_SOM_pcb.hyp TIEplus23_SOM_Assembly_Drawing_Prototype.pdf	Same CAD data in different formats to facilitate importing in different simulation tools
PCB Stack-up	Slide 5	PCB material data
Decoupling Capacitor models	https://www.murata.com/en-eu/products/capacitor/ceramiccapacitor/overview/lineup/smd/grm https://ds.murata.co.jp/simsurfing/index.html?lcid=en-us	GRM Series overview SimSurfing link
Schematic	TIEplus23_SOM_schematic.pdf	
IC2 Renesas SoC documentation	RZG2L_hardware_datasheet.pdf RZG2L_DDR_PCB_verification_guide.pdf RZG2L_pinfunction_List.xlsx	SoC datasheet PCB design verification guide for DDR Pin list
IC4 DDR4 Memory datasheet	16gb_ddr4_sdram.pdf	DDR4 Memory IC datasheet
JEDEC DDR4 Specification	JESD79-4A.pdf	JEDEC specification for DDR4 signaling
RZV2L IBIS model	rzg2l_ibis_ddr.ibs	IBIS model for SoC
DDR4 IBIS model	z22a_ait.ibs	IBIS model for Memory IC
RZ/G2L package s-parameter	RZG2L_DDR_DQ.s68p RZG2L_DDR_CA.s86p RZG2L_DDR_VDDQ.s8p	Memory controller package touchstone model including VDDQ on-die decoupling
DDR4 on-die PDN model	z22a_ondie_decoupling_perdq.ckt z22a_ondie_decoupling_alldq.ckt	Memory IC package model of on-die decoupling for VDDQ
PMIC model	Slide 6	RL modeling of PMIC output impedance
Target Impedance requirement	Slide 7	Target Impedance requirement for DDR4 IC and SoC

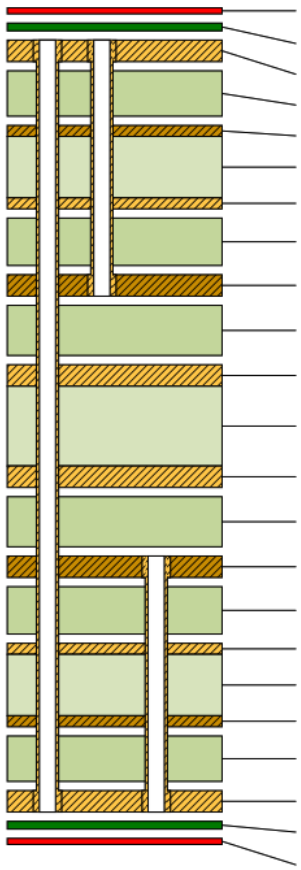
TIEplus 2023
Input Data

TIEplus

› Stack-up

Notes:
1. All layer dimensions specified after pressing
2. Dk, Df values specified at 1GHz

Layer Stack Legend



Material	Layer	Thickness	Type	Gerber	Df	Dk
	Top Overlay		Legend	GTO		
Surface Material	Top Solder	0.013mm	Solder Mask	GTS		3.4
Copper	TOP	0.035mm	Signal	GTL		
Prepreg		*0.074mm*	*Dielectric*		*0.019*	*4.17*
CF-004	GND1	0.018mm	Internal Plane	GP1		
Core		*0.100mm*	*Dielectric*		*0.018*	*4.31*
CF-004	SIG1	0.018mm	Signal	G1		
Prepreg		*0.077mm*	*Dielectric*		*0.02*	*4.02*
CF-004	GND2	0.035mm	Internal Plane	GP2		
Prepreg		*0.082mm*	*Dielectric*		*0.02*	*4.02*
CF-004	PWR1	0.035mm	Signal	G2		
Core		*0.130mm*	*Dielectric*		*0.015*	*4.61*
CF-004	PWR2	0.035mm	Signal	G3		
Prepreg		*0.082mm*	*Dielectric*		*0.02*	*4.02*
CF-004	GND3	0.035mm	Internal Plane	GP3		
Prepreg		*0.077mm*	*Dielectric*		*0.02*	*4.02*
CF-004	SIG4	0.018mm	Signal	G4		
Core		*0.100mm*	*Dielectric*		*0.018*	*4.31*
CF-004	GND4	0.018mm	Internal Plane	GP4		
Prepreg		*0.074mm*	*Dielectric*		*0.019*	*4.17*
Copper	BOT	0.035mm	Signal	GBL		
Surface Material	Bottom Solder	0.013mm	Solder Mask	GBS		3.4
	Bottom Overlay		Legend	GBO		

Total thickness: 1.103mm

TIEplus 2023
Input Data

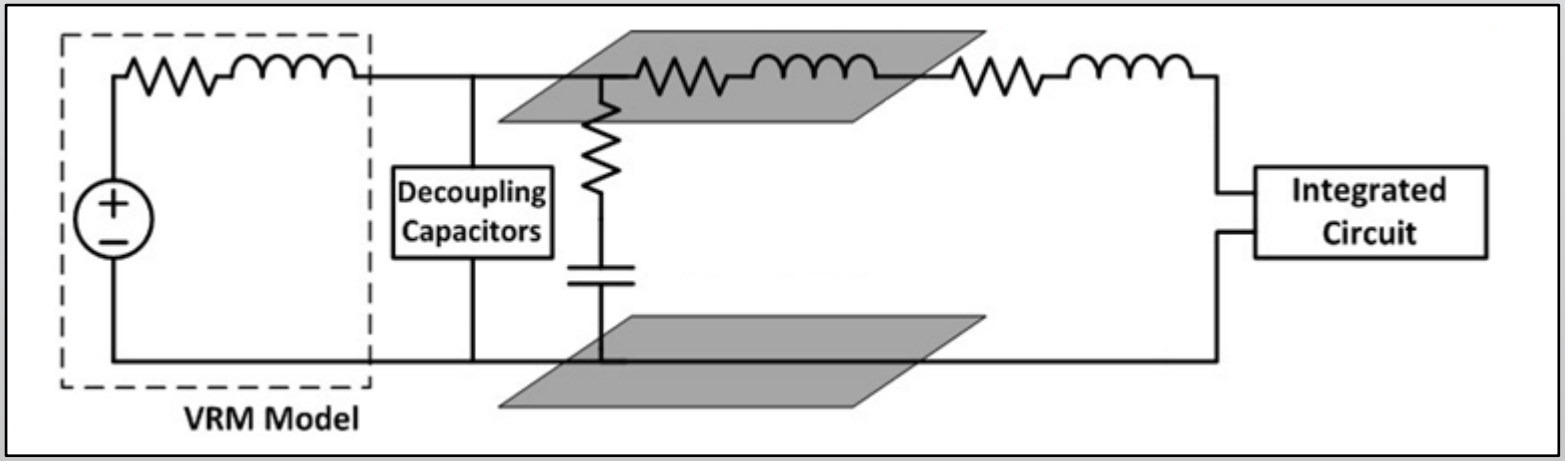
› PMIC Modeling

Output Voltage: 1.2 [V] (net ***1V2_DDR***)

Output Switching Ripple: 9.5 [mV]

Set point accuracy: +/-1.2 %

R_{VRM} = 35 mΩ L_{VRM} = 68 nH



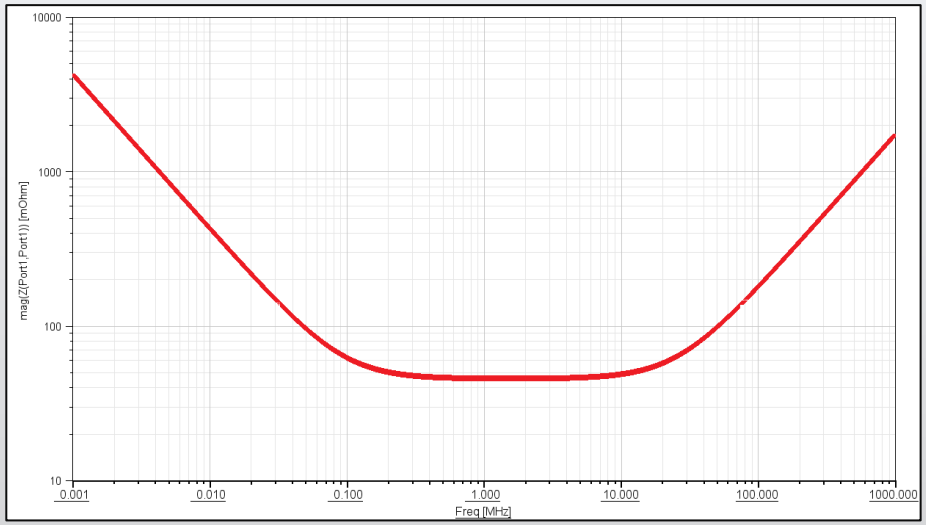
TIEplus 2023
Input Data

› Target Impedance requirement DRAM

VDDQ Supply : 1.2V ±5%

Max. DC current: 0.38 A

Data files:
- DRAM_target.csv
- DRAM_target.s1p



› Target Impedance requirement SoC

Follow PDN verification method described in chapter 6 of „RZG2L_DDR_PCB_verification_guide.pdf" for 1V2_DDR power rail

Max. SoC PDN Target Z definition up to 100MHz →

Table 6.1 Target impedance for SoC IO PDN

	Target impedance: Ztarget(f)		
Frequency	Min	Max	Unit
100kHz – 10MHz	—	0.05	Ω
10MHz – 20MHz	—	0.08	Ω
20MHz <	—	0.32	Ω