UNIVERSITATEA LUCIAN BLAGA DIN SIBIU

"Lucian Blaga" University of Sibiu
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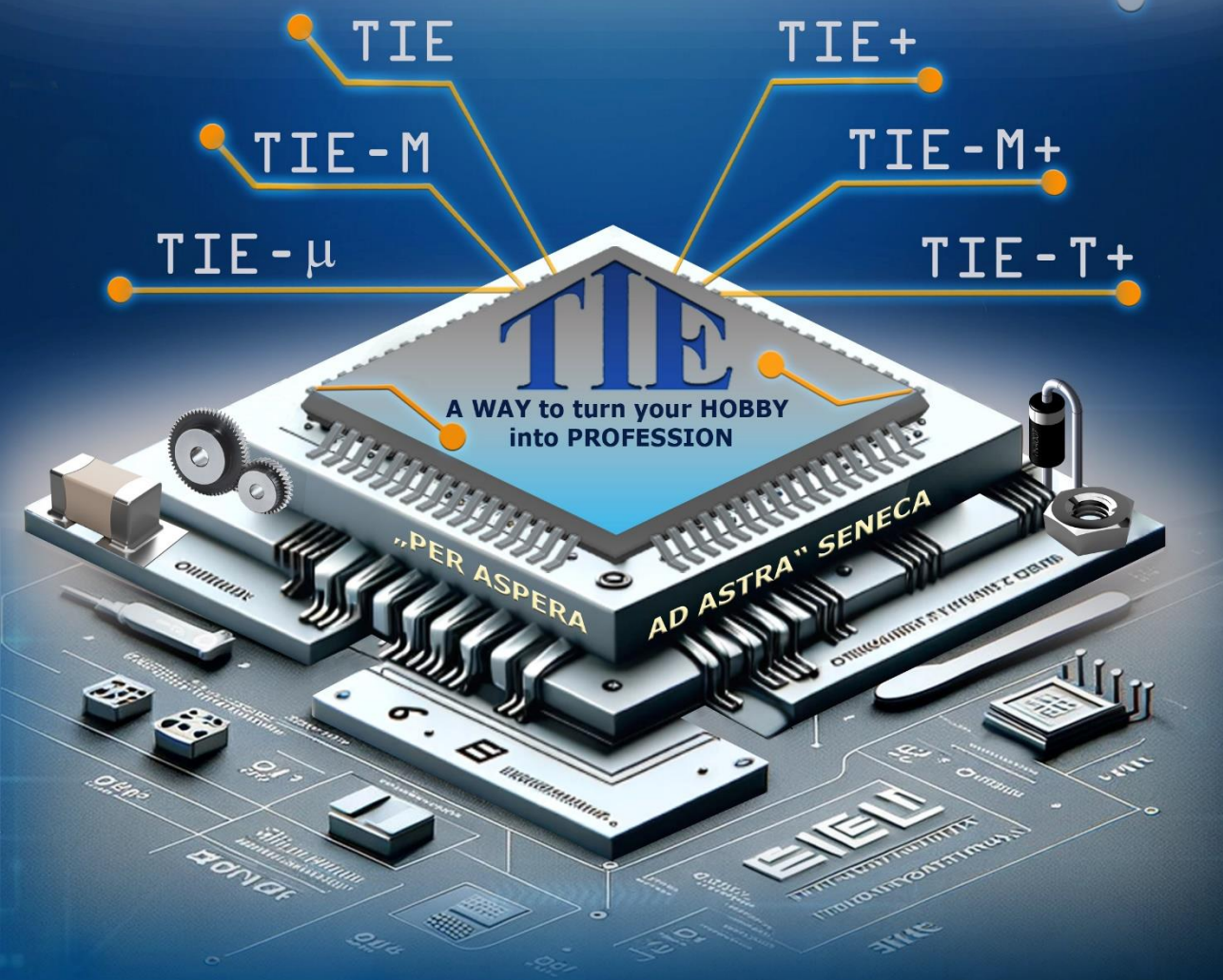
POLITEHNICA BUCUREȘTI 205 ANI DE INOVAȚIE 1818 UNST

TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS (TIE)



Sibiu, Romania

24 - 27 April 2024

Organized by:

National University of Science and Technology POLITEHNICA Bucharest, Romania
http://www.upb.ro

Faculty of Electronics, Telecommunications and Information Technology
https://etti.upb.ro/

Faculty of Mechanical Engineering and Mechatronics
http://www.mecanica.pub.ro

Lucian Blaga University of Sibiu, Romania
https://www.ulbsibiu.ro/en/

Faculty of Engineering
https://inginerie.ulbsibiu.ro/

Association for Promoting Electronics Technology APTE, IMAPS Chapter Romania
http://www.apte.org.ro

Continental Automotive Systems Sibiu, Romania
https://www.continental.com/

Center for Technological Electronics and Interconnection Techniques
http://www.cetti.ro

and supported by:

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DTP: Bogdan Mihăilescu
Publisher: Cavallioti

TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS, an Electronics Packaging Specialized Event

A WAY to turn your HOBBY into PROFESSION

TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS

TIE, 33rd Edition

PROFESSIONAL STUDENT CONTEST

Lucian Blaga University of Sibiu,

April, 24 – 26, 2024

THE PROFESSIONAL STUDENT CONTEST

TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS - 2024

Program Brochure

Welcome to TIE 2024 Event

The current TIE edition was able to return to the format and time season established by the previous editions of the pandemic, offering hobbyist students in the field of electronic packaging to face the rigors required by the industry regarding the design of an electronic package.

In the book *Electronic Packaging, Microelectronics, and Interconnection Dictionary*, edited by **Charles Harper and Martin Miller** and published by McGrow-Hill, Inc., it is specified: **Electronic Package** *The electro-mechanical assembly resulting from electronic packaging design and manufacture. The level of an electronic package may range from the integrated circuit package assembly to a printed wiring board assembly to a subsystem or system package assembly. And* ***Electronic Packaging*** *is defined as the engineering discipline that combines the engineering and manufacturing technologies required to convert an electrical circuit into manufactured assembly. These include at least electrical, mechanical, and material design and many functions such as engineering, manufacturing, and quality control.*

The recent TIE edition, which can rightly be considered a true electronic packaging specialized event, brings together six topics. These consider both electrical aspects (TIE E, TIE E+, TIE u) and non-electrical aspects (TIE M, TIE M+, TIE T+).

Like the previous TIE editions, the topics offered to students for solving are concepted and developed by specialists from the electronic industry present in Romania.

I would like to take advantage of the front lines to thank companies such as Continental Automotive Romania, Marvell Technology Romania, as well as Microchip Technology Romania for their major involvement in the preparation of the subjects.

Of course, the entire event could not have taken place at such a high level of complexity as the current one if we had not had special support from the organizers Lucian Blaga University of Sibiu, Continental Automotive System srl Romania, Sibiu, as well as numerous specialists from the electronics industry, people who are nominated in the brochure of the recent TIE edition.

Moreover, following the evolution of numerous TIE editions, it can be noted that this event is more and more in line with the normality required by the education and training of students, future engineers. The close collaboration between academia and industry is a very good guarantee of future engineers' ability to be competitive in their future

profession. The skills acquired by students through TIE represent today a very good mix between the theoretical aspects, acquired during university studies, and those specific to the engineering profession, according to the electronic packaging requirements. This binomen, Education-Industry, of shaping of a future engineer represents the key element in creating the needed workforce necessary for growing of an industry, the electronic one, with such a large impact for the prosperity of a society. In fact, many decades ago, **Prof. Rao Tumala,** Georgia Institute of Technology, USA, had mentioned in one of his books, Fundamentals of Microsystems Packaging: *The global electronic industry acts as the engine for science, technology, advanced manufacturing, and the overall economy of the countries that participate in it.*

Finally, I would like to thank all the people involved in organizing the current TIE edition, Sponsors, and Exhibitors, without whom the existing high level could not have been ensured. The brochure offers all the information needed to obtain a well-established image regarding the community that promotes electronic packaging education and training development. Many thanks!

For all TIE participants: I wish you to have many fruitful discussions and a very pleasant stay in Sibiu.

Prof. D.H.C. mult. Paul SVASTA, Ph.D.
National University of Science and Technology
POLITEHNICA of Bucharest, Romania
APTE-Association for Promoting Electronics Technology
TIE General Chair

Prof. Ovidiu POP, Ph.D.
Technical university of Cluj-Napoca
TIE General Chair

Dear participants and guests,

On behalf of the local organizing committee, I am delighted to welcome you all to Sibiu for the 2024 chapter of the Technologies of Interconnection in Electronics (TIE) event.

Returning to the picturesque city of Sibiu after 12 years, the event has since grown to include 6 separate competitions, all distinct but also all tied to and covering different aspects of electronic packaging. Along with the classic PCB design contest TIEE, which is at its 33rd edition, the event includes the 3rd edition of TIEM for mechanical design, the advanced analysis contests TIEE+ (8th edition) and TIEM+ (2nd edition), as well as the first editions for TIET+ (thermal) and TIEμ (microelectronics).

TIE is much more than a simple academic competition, it is an excellent meeting point of industry and education, and a great chance for students to experience realistic demands and take first steps towards a fulfilling carrier.

Hoping you will have a enjoyable stay, not only because of the new knowledge shared here, I am looking forward to creating together a very successful event!

Prof. Maria VINŢAN, Ph.D.
Dean of the Faculty of Engineering,
Lucian Blaga University of Sibiu
TIE 2024 Chair

Quo vadis TIE?

With a long tradition of more than 25 years, the student design competition for the electronics industry has evolved in recent years into an integrated platform for professional development, and not just for students. However, if preparing students for the tough professional life of today's world, especially in a hyper-competitive field such as electronic systems development and applications that massively embed the electronic product, is at the heart of this event, other equally relevant gains should not be neglected. By the specificity of this event, of establishing competition themes through close collaboration between former students - now members of the engineering body in companies or higher education institutions, a forum is generated in which current engineering requirements, communicated and explained by design engineers, reach the teaching staff, allowing an understanding of training needs and a scaling, improvement or even "reinvention" of some disciplines. Moreover, on these occasions, discussions are initiated that lead to far-reaching changes, not only to the subject sheets, but even to the curricula. New specializations, new curricula and the development of new forms of training with a strong theoretical-applied education synergy, such as dual or short-term education, were also initiated during this period. This exhaustive but detailed interaction between the educational area and the industrial design area has effects in both directions, not limited to the educational environment. Industry specialists have the opportunity, when proposing and discussing topics, to receive information from professors on the current level of training, on mentalities and on validated ways of stimulating to increase the efficiency of the training of young engineers, valuable information because university training is only a basic training, which will be used, improved and even profoundly rewritten, in times of disruptive transformations, during the professional career in companies.

This "agora" of electronics in Romania - TIE, has expanded in recent years as a result of the regeneration of the electronics industry and the permanent evolution in recent decades, from a focus on production to design, development and even, in the case of some companies, research. The development in Romania of very complex electronic and mechatronic products, in the automotive, space/aeronautics and medical fields, has required the solution to complex problems, interconnected with the purely electronic, "mechanical" development issues, from the optimal design of the support, protection and sometimes actuation structures associated with PCBs, down to the solution of complex thermo-mechanical behavior requirements in quasi-static but also dynamic conditions. The TIE-M branch for optimal geometrical design has emerged organically, closely related to the specific constraints of the electronic product but also of its integration in a

functional assembly. The natural step was to address the aspects of mechanical deformation under the effect of external loads (inertial effects, clamping forces) but also mechanical stresses due to temperature variations in the system. The development of a functional system for the automotive field, characterized by strict reliability requirements under very complex demands, is not possible without a dynamic analysis. Consequently, TIE-M Plus resulted as a verification of the highest level of mechanical design skills.

In its first generations in extended format, after a long tradition in purely electrical design, the TIE-M and TIE-M Plus competence will certainly have a favorable but challenging future, with new exciting provocations expected from the move to the micro level, as well as the need to move from sequential to parallel design, with simultaneous integration of electrical and electromagnetic, mechanical, thermal and possibly linked physical phenomenon aspects.

Prof. Daniel COMEAGĂ, Ph.D.
National University of Science and Technology
POLITEHNICA of Bucharest, Romania
TIE_M Chair

TIE-M competition

The end of 2021 marked the year when I joined the TIE ecosystem, laying the groundwork to launch the first edition of TIE-M in the fall of 2022, a cutting-edge mechanical design contest that emphasizes the importance of mechanical design for electronic modules. Drawing from my professional experience in electronic module design for automotive applications, I recognized early on the significance of robust design and its impact on the reliability of electronic modules during operation. Industrial and academic peers responded promptly to the call by hosting the TIE-M event annually since then, with more than 15 students participating each year.

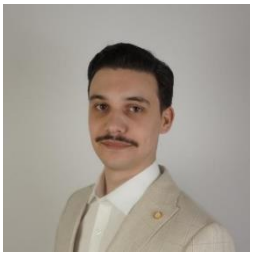
TIE-M competition focuses on applying the accumulated knowledge of participants, with four hours allotted for contestants to solve the subject matter, which includes questions on design, manufacturing technologies, and 2D drawing.

But that's not all. As engineering advancements propel us forward, the design of a module is just the beginning—it must also undergo validation. Thus, TIE-M Plus and TIE-T Plus were born.

In collaboration with colleagues from the expert community, we established two contests for advanced simulation: one focusing on Structural Analysis of electronic modules, and the other on Thermal Management. Both are of utmost importance given the latest trends in electronic packaging.

The advanced simulation competitions follow a different format, with a series of workshops and training sessions offered to participants prior to the subject release. Participants then have a two-week period to solve the subject, with regular meetings set with the technical committee to address any potential roadblocks. For the final evaluation of solutions, a public defense of the presentation is scheduled, during which contestants must justify their approach in a live discussion with professionals from academia and industry.

Considering this, I believe that the newly added sessions of the TIE platform have already matured, evident in the interest shown by academia and industry in the mechanical, structural, and thermal challenges related to electronic modules. These sessions focus on both design and validation, encompassing the main disciplines involved in the development process.



Philip COANDA
System Design Engineer
Continental Automotive Timisoara

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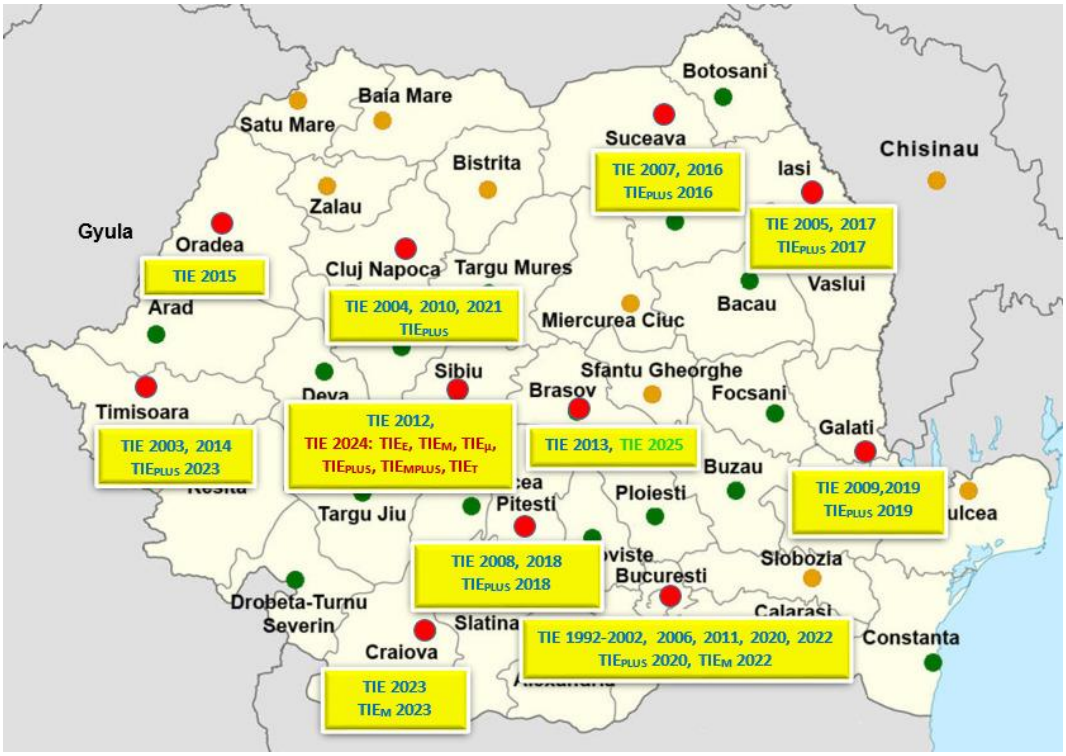
TIE 2024 Agenda

Wednesday, April 24		
09:00 – 19:00	Registration	Hall of the Faculty of Medicine
10:00 – 11:00	Welcome speech	Library, 3rd floor hall
11:00 – 12:00	Technical meeting TIE_{EPLUS}, TIE_{MPLUS}, TIE_{TPLUS}, TIE_{μ}	Library, 3rd floor hall
12:00 – 13:00	*Lunch*	*Library, Private Area (ground floor)*
13:00 – 17:00	TIE_{EPLUS} Contest	Library, Internet Room (ground floor)
13:00 – 17:00	TIE_{MPLUS} Contest	Library 3rd floor hall
13:00 – 17:00	TIE_{TPLUS} Contest	Library, Room 314 (3rd floor)
17.00 – 17.15	*Coffee Break*	*Library, Private Area (ground floor)*
17:15 – 18:00	TIE_{EPLUS} Committee Assessment meeting	Library, Internet Room (ground floor)
17:15 – 18:00	TIE_{MPLUS}Committee Assessment meeting	Library, Multimedia Room (3rd floor)
17:15 – 18:00	TIE_{TPLUS}Committee Assessment meeting	Library, Room 314 (3rd floor)
18:15 – 19:30	Steering Committee Meeting	Library, Room 314 (3rd floor)
21.00	*Dinner*	*My Continental Hotel*
Thursday, April 25		
08:15 – 14:00	Welcome & Registration	Hall of the Faculty of Medicine
08:45 – 10:45	CAD Activities in Education and Training - WORKSHOP on Multiphysics Approach	Aula Magna
10.45 – 11.00	*Coffee Break*	*Library, Private Area (ground floor)*
11:00 – 12:00	CAD Activities in Education and Training - WORKSHOP on Multiphysics Approach	Aula Magna
12:00 – 13:00	*Lunch*	*Library, Private Area (ground floor)*

TIE 2024 Agenda

13:00 – 16:00	TIEμ contest – First edition	Library, Room 314 (3rd floor)
16.00 – 16.15	*Coffee Break*	*Library, Private Area (ground floor)*
16:15 – 17:00	TIEμ Committee Assessment meeting	Library, Room 314 (3rd floor)
17:00 - 18:00	Industrial Session	Aula Magna
17:00 - 18:00	Steering Committee Meeting	Library, Internet Room (ground floor)
18:00 – 19:00	Awarding TIEplus's and TIEμ	Aula Magna
19:00 – 20:30	Technical meeting TIE_E, TIE_M	Aula Magna
21:00	*Dinner*	*My Continental Hotel*
Friday, April 26		
07:30 – 08:00	TIE_E, TIE_M preliminary activities	Library 3rd floor hall Library, Internet Room (ground floor)
08:00 – 12:30	TIE_E contest	Library 3rd floor hall
08:00 – 12:30	TIE_E committee evaluation scaling	Library, Room 314 (3rd floor)
08:00 – 12:30	TIE_M contest	Library, Internet Room (ground floor)
08:00 – 12:30	TIE_M committee evaluation scaling	Library, Private Room (ground floor)
12:30 – 13:30	*Lunch*	*Library, Private Area (ground floor)*
13:30 – 18:00	Assessments	Library, 3rd floor hall, Internet Room
18:00 – 19:00	Steering Committee Meeting	Aula Magna
19:30– 20:30	Awarding TIE_E, TIE_M	Aula Magna
21.00	*Gala dinner*	*My Continental Hotel*
Saturday, April 27		
09:00	Sibiu City Tour	

TIE & TIE$_M$ & TIE$_{PLUS}$ past, present and future editions



Year	University	Event
1992-2002	University Politehnica of Bucharest	TIE
2003	Politehnica University of Timişoara	TIE
2004	Technical University of Cluj-Napoca	TIE
2005	Gh. Asachi Technical University of Iaşi	TIE
2006	University Politehnica of Bucharest	TIE
2007	Ştefan cel Mare University of Suceava	TIE
2008	University of Piteşti	TIE
2009	Dunărea de Jos University of Galaţi	TIE
2010	Technical University of Cluj-Napoca	TIE

TIE & TIE$_M$ & TIE$_{PLUS}$ past and present editions

2011	University Politehnica of Bucharest	TIE
2012	Lucian Blaga University of Sibiu	TIE
2013	Transilvania University of Braşov	TIE
2014	Politehnica University of Timişoara	TIE
2015	University of Oradea	TIE, TIE$_{Plus}$ Kick-off
2016	Ştefan cel Mare University of Suceava	TIE, TIE$_{Plus}$
2017	Gh. Asachi Technical University of Iaşi	TIE, TIE$_{Plus}$
2018	University of Piteşti	TIE, TIE$_{Plus}$ 1st TIE bootcamp
2019	Dunărea de Jos University of Galaţi	TIE, TIE$_{Plus}$
2020	University Politehnica of Bucharest - Virtual Event	TIE, TIE$_{Plus}$
2021	Technical University of Cluj-Napoca - Virtual Event	TIE, TIE$_{Plus}$
2022	University Politehnica of Bucharest	TIE, TIE$_M$ Kick-off
2023	University of Craiova	TIE, TIE$_M$
	Politehnica University of Timişoara	TIE$_{Plus}$, TIE$_M$ $_{Plus}$
2024	Lucian Blaga University of Sibiu Continental Automotive Sibiu	TIE$_E$, TIE$_{Plus}$, TIE$_M$, TIE$_M$ $_{Plus}$, TIE$_T$, TIE$_\mu$
2025	Transilvania University of Braşov	TIE$_E$, TIE$_{Plus}$, TIE$_M$, TIE$_M$ $_{Plus}$, TIE$_T$, TIE$_\mu$

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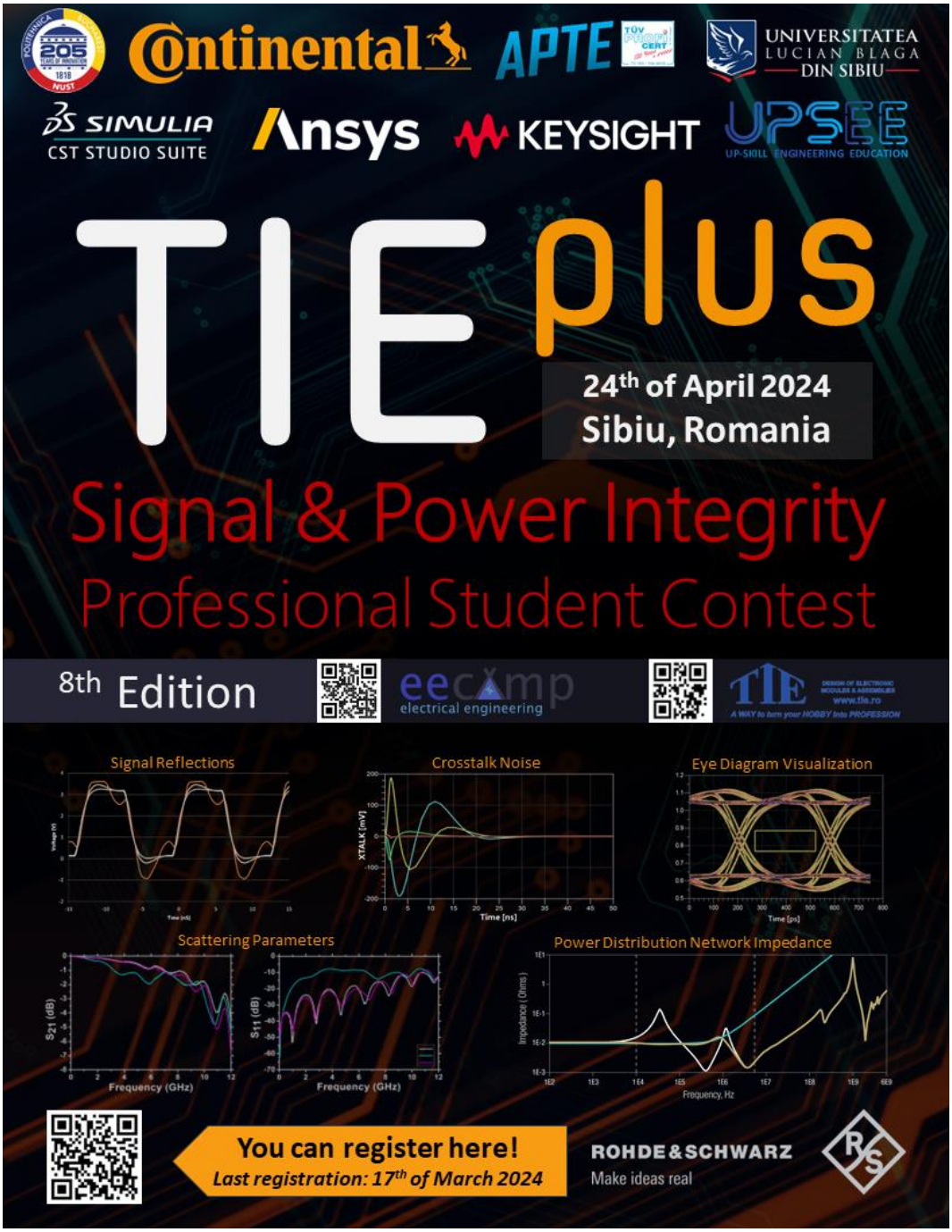
21.00	*Dinner*	*My Continental Hotel*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Professional Student Contest
8th Edition
eecamp
electrical engineering
TIE
Signal Reflections
Crosstalk Noise
Eye Diagram Visualization
Scattering Parameters
Power Distribution Network Impedance
Frequency (GHz)
Frequency (GHz)
Frequency, Hz
You can register here!
Last registration: 17th of March 2024
ROHDE&SCHWARZ
Make ideas real

TIE $_{E+}$ – Propagating excellence since 2015

Launched in 2015, TIE$_{E+}$(TIE-E PLUS) represents an evolutionary extension of the TIE brand, focusing on virtual prototyping disciplines essential for managing the complexities of high-end PCB designs. This initiative is a strategic progression aimed at fostering PCB design expertise within the Romanian electronics community. Building on the foundational knowledge acquired in the TIE$_{E}$(TIE-E) contest, which covers the intricacies of PCB layout interconnect design, TIE$_{E+}$ shifts the spotlight to the critical analysis of signal and power integrity across these interconnects. Contestants are tasked with generating both pre-layout recommendations and post-layout evaluations of a given electronic module, thus demonstrating a deeper engagement with the engineering design process.

More than a competition, TIE$_{E+}$ is a comprehensive educational platform that encourages students to not only assimilate new knowledge but polish highly sought-after skills. Defending their design solutions before the TIE$_{E+}$ committee offers a unique opportunity for participants to enhance their analytical abilities and refine their presentation and discussion skills. This interaction underlines the multifaceted nature of PCB design, requiring a balance between performance, design constraints, and cost considerations – factoring in the technology employed in PCB fabrication and the design resources at hand.

The TIE$_{E+}$ competition unfolds through a structured sequence of steps, designed to facilitate an engaging and educative experience for the students, while trying to emulate the typical engineering design process prevalent in the electronics industry:

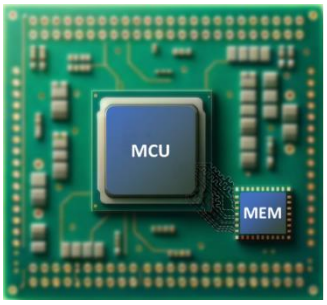

Figure 1 Subject theme

- Subject Announcement – An overview of the TIE$_{E+}$ theme and main topics of the subject are made available online. This gives students ample opportunity to deepen their understanding of the specific protocols or technologies.
- Student Enrollment – The committee conducts a thorough review of all registration submissions to ensure a level playing field. Candidates with extensive experience in SI/PI are carefully screened to maintain the competition's focus on developing talent.
- Challenge Resolution – Participants are granted a two-week period to solve the given challenge and craft their technical solutions, submitted in the form of an R&D report.
- Solution Evaluation – Following submission, contestants are expected to prepare and deliver a concise presentation (lasting 15-20 minutes) to the technical committee.

This approach not only prepares participants for the rigorous demands of the electronics design industry but also ensures that each phase of the competition is an opportunity for learning, skill enhancement, and meaningful feedback, underscoring the competition's role as a bridge between academic learning and professional application.

The core challenge lies in effectively integrating signal integrity (SI) analysis with power distribution network (PDN) considerations. This involves ensuring that signals are transmitted with minimal distortion and interference, while also managing the power delivery to all the components in the system, to guarantee stable and reliable operation.

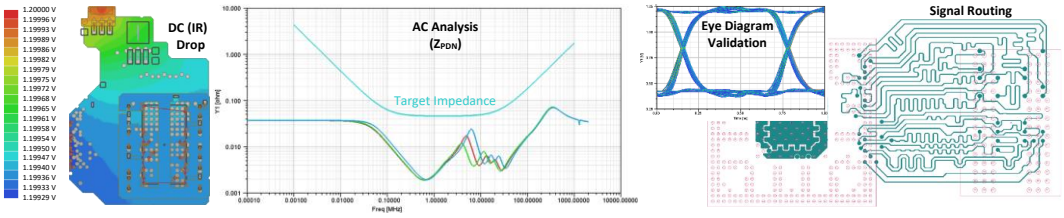

Figure 2 Subject highlights

In the evaluation phase of the contest, a panel comprised of experts from both the industrial sector and academic institutions comes together to meticulously review the R&D reports submitted by contestants. Prior to the oral presentations, each evaluator dedicates time to thoroughly examine the reports, formulating precise inquiries focused on the methodology and clarity of the results derived from the simulation processes. The evaluation is structured around three core competencies:

- Software Proficiency – Examining the participant's ability to effectively employ the available simulation tools and configure the appropriate settings for accurate results.
- Theoretical Insight – Assessing the contestant's understanding of the physical principles and phenomena that are fundamental to the topics being investigated.
- Solution Excellence – Evaluating the originality, practicality, and technical soundness of the proposed solution, including how well it addresses the challenge presented.

To be recognized by the TIE$_{E+}$ committee as proficient in the SI/PI domain and to be awarded a diploma, participants must demonstrate broad understanding across a wide array of topics and successfully address more than half of the subject requirements. This process ensures a rigorous standard of competence and also mirrors the professional evaluation methodologies used in industry and academia, fostering a realistic and constructive environment for learning and recognition.

***Marcel Manofu**, Continental Automotive Romania, Timișoara*

***Mihai Dărăban**, Technical University of Cluj-Napoca*

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Mihai RUS, Continental Engineering Services
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TIE-M+ – Accept the Structural Challenge

Finite element analysis (FEA) is a numerical method used for predicting how an object or an assembly behaves under given physical conditions.

It is necessary to use mathematics to comprehensively understand and quantify any physical phenomena such as solid mechanics, fluid mechanics, electromagnetics, heat transfer, acoustics, or other physical effects.

Most of these phenomena are described using Partial Differential Equations (PDEs). Solving these PDEs, even by using computational methods, required the development of specific numerical techniques over the last few decades, out of which a prominent one is the FEA.

Engineers in various industries heavily rely on FEA, because of its benefits including increased accuracy of prediction, better insight into critical design parameters, virtual prototyping, fewer hardware prototypes and experimental validations, a faster and less expensive design cycle, increased productivity, and, overall, an increased revenue.

Starting from 2023, TIE introduced a new section called TIE-M+, focusing on structural and thermal management analysis of electronic packaging. The contest provides students with a comprehensive electronics development experience concerning structural integrity aspects. Organizing such a FEA competition in Romania helps to fill the gap in a multidisciplinary contest, offers an opportunity for students to relate their theoretical knowledge to practical examples, and helps to bring together specialists and experts from the industrial and academical partners.

The subjects the students must develop are focusing on different types of electronic modules, such as particular control units or sensors, coming from the forefront of the automotive industry, including business areas like Architecture and Networking or Autonomous Driving.

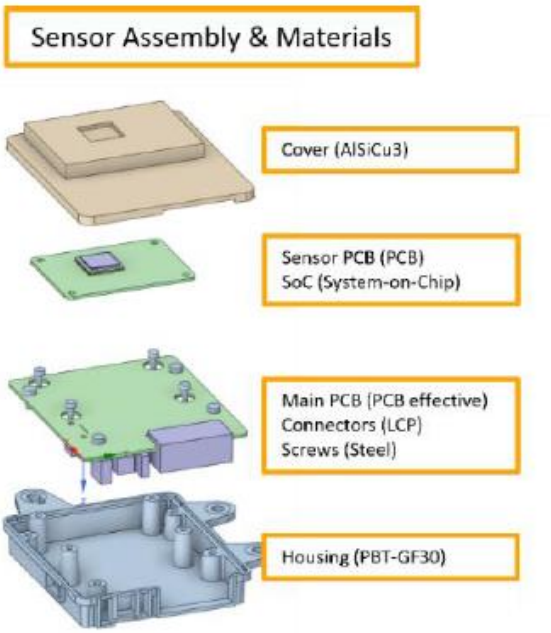

Figure 1 *Example of a product chosen for the simulation contest*

The goal is to have the students understand the product and its weak spots, properly design a path towards its numerical evaluation (e.g., PCB deformation, natural frequency, and mode shape analysis) and give recommendations for design optimizations to improve system performance.

The general objective of the structural simulation contest is to familiarize the students to the basic knowledge regarding numerical simulations. In addition to this, a specific objective is to familiarize the contestants to the state-of-the-art practical workflows used within industry, to prepare the future engineers for a career in the structural simulation field.

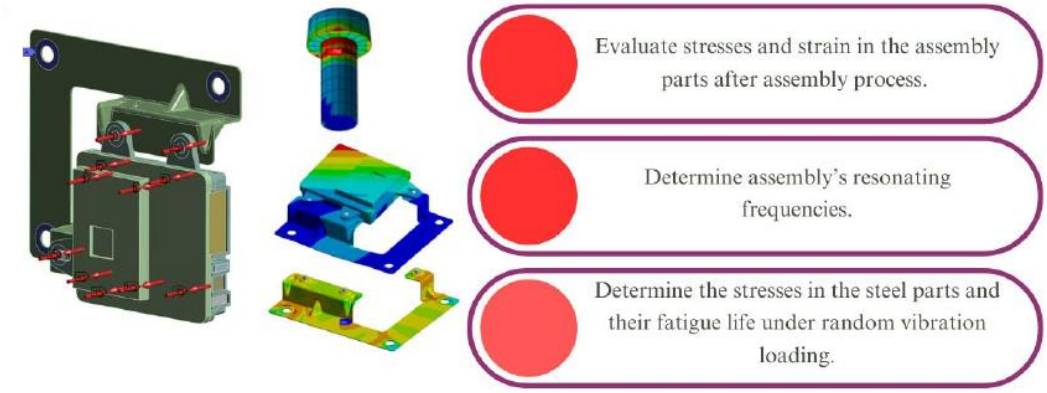

Figure 2 *Numerical model and the corresponding subjects required*

Tamas Krausz*, Continental Automotive Romania*

Ștefan Sorohan*, POLITEHNICA Bucharest, Romania*

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Marius POPUȚOAIA, Continental Automotive System Sibiu
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TIE-T+ Iterative Design and Optimization

Thermal management optimization is an iterative process that requires multiple rounds of simulation, testing, and refinement. As new components or cooling technologies are introduced, the thermal management system must be continuously evaluated and optimized to ensure it can handle the evolving heat loads and maintain the desired performance and efficiency targets.

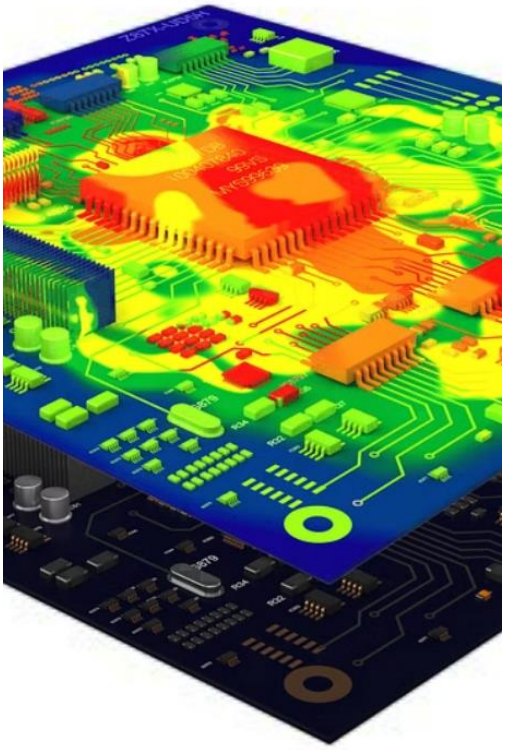
Choosing the most appropriate cooling method, such as active or passive cooling, is key to optimizing thermal performance. Simulation and modeling can help engineers evaluate the effectiveness of different cooling solutions and select the most suitable approach for their specific application.

Simulation and modeling can help evaluate and refine initial thermal management concepts. By virtually testing different design ideas, engineers can identify the most promising approaches and make informed decisions before investing in physical prototypes, leading to a **more efficient and cost-effective design** process. As computational power and algorithm sophistication improve, engineers will have access to more advanced tools to tackle increasingly complex thermal management challenges.

The Role of Simulation and Modeling

Predictive Capabilities

Simulation and modeling allow engineers to predict thermal behavior and identify potential hot spots before physical prototyping. By virtually testing various design scenarios, engineers can gain valuable insights into the thermal performance of their systems, enabling them to make informed decisions and optimize the design before investing in physical hardware.



Optimization Opportunities

These simulation and modeling tools enable designers to explore a wide range of design options and find the most optimal thermal management solutions. By comparing the

thermal performance of different cooling techniques, component placements, and airflow patterns, engineers can identify the most efficient and cost-effective approach to maintain the desired operating temperatures within their electronic devices.

Reduced Costs

Simulation and modeling can significantly reduce the need for costly physical testing and iterations. By identifying and resolving potential thermal issues early in the design process, engineers can minimize the number of physical prototypes required, saving time and resources. This approach allows for a more streamlined and efficient product development cycle, ultimately leading to faster time-to-market and reduced overall costs.

Integrated Multiphysics

The integration of thermal management with other physical domains, such as electromagnetics and structural mechanics, will become increasingly important. By considering the interactions between these different phenomena, engineers can develop a more comprehensive understanding of the system's behavior and optimize its performance more effectively.

***Cristina Mihaela Dragan**, Continental Automotive Romania*

***Ciprian Ionescu**, POLITEHNICA Bucharest, Romania*

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Thursday, April 25		
08:15 – 19:00	Welcome & Registration	Hall of the Faculty of Medicine
08:45 – 10:45	CAD Activities in Education and Training - WORKSHOP on Multiphysics Approach	Aula Magna
10.45 – 11.00	*Coffee Break*	*Library, Private Area (ground floor)*
11:00 – 12:00	CAD Activities in Education and Training - WORKSHOP on Multiphysics Approach	Aula Magna
12:00 – 13:00	*Lunch*	*Library, Private Area (ground floor)*
13:00 – 16:00	TIEμ contest – First edition	Library, Room 314 (3rd floor)
16.00 – 16.15	*Coffee Break*	*Library, Private Area (ground floor)*
16:15 – 17:00	TIEμ Committee Assessment meeting	Library, Room 314 (3rd floor)
17:00 - 18:00	Industrial Session	Aula Magna
17:00 - 18:00	Steering Committee Meeting	Library, Internet Room (ground floor)
18:00 – 19:00	Awarding TIEplus's and TIEμ	Aula Magna
19:00 – 20:30	Technical meeting TIE$_E$, TIE$_M$	Aula Magna
21:00	*Dinner*	*My Continental Hotel*

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1st edition
25th of April 2024
Sibiu, Romania
Take on the Advanced Packaging Challenge
in Our First Chiplet-Interconnect Dedicated Contest
Interconnections
Standards
Signal Integrity
Individual chip testability
Advanced Packaging

TIE-μ – a new TIE topic launching in 2024

Gordon Moore famously predicted in his" Moore's Law" paper that it might become more cost-effective to construct extensive systems using smaller, individually packaged functions interconnected together. More than half a century later, the structure of the System-on-a-Chip (SoC) changes significantly with the partitioning of a monolithic die into smaller chiplets: packaging becomes one of the main focuses when designing a chip and the way the initial functionality is partitioned between multiple chiplets and how these are interconnected means we must shift our perspective to Systems in Package (SiP) (source: A. Jâjâie, A. Puşcaşu, I. Ailenei, C. B. Ciobanu and P. Svasta, "Chiplets and Next-gen Packaging Technologies in University Education," 2023 IEEE 29th International Symposium for Design and Technology in Electronic Packaging (SIITME), Craiova, Romania, 2023, pp. 207-214, https://doi.org/10.1109/SIITME59799.2023.10431355)

As the industry shifts towards heterogeneous integrations, systems in package and chiplets it becomes of paramount importance to train future engineers in these state-of-the-art techniques, including employing interposers, 2.5D, and 3D integration.

Starting from this year, TIE introduces a new topic – TIE-μ, which is addressing important subjects such as advanced packaging, 2.5D/3D integration and chiplets. In this regard, TIE is a unique approach and to our knowledge the only one of this type in Europe which bridges the gap between Universities, Industry and advanced topics such as Chiplets as shown in Figure 1. The contest brings all stakeholders to the table, ensuring industry relevant data sets are proposed as topics using state of the art EDA tools in an academic environment, in order to introduce future engineers to an upcoming future career path in advanced packaging, chiplet integration and heterogenous design.

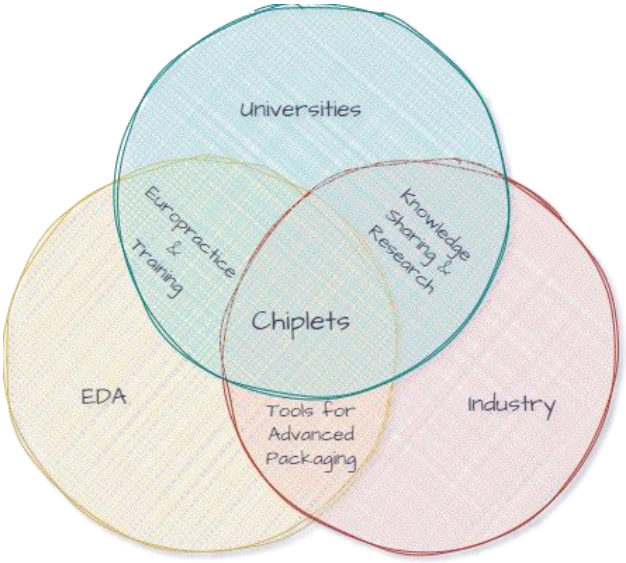

Figure 3 *Interaction between Industry, Universities and Chiplets*

As illustrated in Figure 2 (source: https://www.nature.com/articles/s41928-024-01126-y), the modern approach for heterogenous integration requires high speed interfaces such as Universal chiplet interconnect express (UCIe) and advanced packaging. TIE-µ focuses on the new interconnection challenges for high-speed interfaces, interposers and other techniques the students need to prepare for when transitioning from SoC to SiPs. SiPs make use of specialized chiplets with customer IP and memory on the same package.

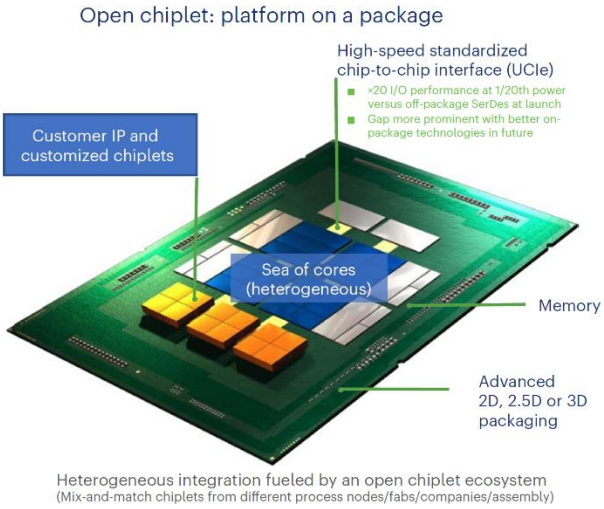

Figure 4 *Heterogeneous open chiplet on-package*

Dan Manolescu, *Marvell Technology*

Cătălin Ciobanu, *Transilvania University of Brașov*

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08:45 – 12:00 CAD Activities in Education and Training - WORKSHOP on Multiphysics Approach

(Library – Aula Magna)

Welcome

Ovidiu Aurel POP, Technical University of Cluj-Napoca, Romania

Cosmin MOISA, Continental Automotive Romania

Moderators:

Paul SVASTA, POLITEHNICA Bucharest

Philip COANDĂ, Continental Automotive Romania, Timișoara

"IC Packaging and Heterogenous Integration"

Syhem LARGUECH, Cadence Design Systems, Application Engineer

"Overcome electronic package design challenges"

Ioan-Alexandru MIHĂILĂ, INAS SA Craiova

Radu-Andrei VĂDUVA, INAS SA Craiova

"How to enable tomorrow workforce to answer the semiconductor Eco System needs"

Catherine LE LAN, Synopsys France, University Program Manager - EMEA

"Advancing Engineering Education: Developing Multiphysics Competency for Electronic Packaging Design"

Marcel MANOFU, Continental Automotive, Timişoara

"Science Parks: Implementation needs in IPCEI RO and Chips Act FI vs. 7th Annual HIR Workshop February 2024"

Cosmin MOISĂ, Continental Automotive, Timişoara

"The Advanced Packaging Master Plan for Europe"

Paul SVASTA, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology

Bogdan MIHĂILESCU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology

PACK4EU

IPCEI on Microelectronics

Name: **Syhem LARGUECH**
Job position: **Application Engineer**
Company: **Cadence Design Systems**
e-mail: **syheml@cadence.com**
Presentation: **"IC Packaging and Heterogenous Integration"**

Syhem LARGUECH received the Dipl.-Ing. degree in electrical engineering from the National Engineering School of SFAX (ENIS), Sfax, Tunisia, in 2012. She earned a PhD degree in Microelectronic Systems from the University of Montpellier, Montpellier, France, in 2015. In 2016, she joined the Interuniversity Microelectronics Centre (IMEC), where she was involved in IC package design and electrical analysis for various applications such as space and high speed. Since September 2019, she has been with Cadence Design Systems in Munich, Germany, where she currently works as an application engineer, supporting Cadence users in the development of their IC packaging projects. She is also actively engaged in the design of advanced IC packages for Cadence's internal hardware products, such as the Palladium platform. Her primary interests revolve around advanced IC packaging technologies, modelling of IC packaging structures, and multi-fabric co-design automation.

Abstract:
IC package is a device used to protect the Integrated Circuit from the outside world. It is considered as sensitive and expensive piece that should not be exposed to the outside. There are a large variety of packages in the market, the lead frame based, the substrate based, the Wafer level based and the advanced packages. In the package, the die is connected to the substrate using wire bonding or Flip chip technology. In the case of Wafer Level Package, redistributed layers are build directly on top of the wafer instead of the die being attached to it using flip chip method.
The semiconductor industry is moving from monolithic chips to the world of 3D-IC, chiplets and stacked silicon and wafers. Advanced systems-on-chip (SoCs) are reaching reticle size limits, and as many companies now realize, simply following Moore's Law alone (More Moore) is no longer the best technical and economical path forward for the next wave of designs. As we approach the device scaling limitations at advanced nodes, the demand on compute performance and data transfer is at an all-time high. There has been a need to find innovative solutions to continue Moore's law scaling and achieve performance improvements with reduced power.
The semiconductor packaging industry is now poised to take on a larger, more significant role in electronic product design of the future. Stacking chips in the same package (3D) and a multi-chiplet system with silicon interposer on the same package (2.5D) are emerging as solutions of choice, which come with their own challenges.

Name: **Catherine LE LAN**
Job position: **University Program Manager - EMEA**
Company: **Synopsys France**
e-mail: **cfranssu@synopsys.com**
Presentation: **"How to enable tomorrow workforce to answer the semiconductor Eco System needs"**

Catherine's experience focuses on worldwide customer success management, encompassing technical customer support, training, projects, and team management.
She holds a master's degree in Microelectronics from ESIEE Paris. She started her career as a Field Application Engineer, progressing to roles as a Technical Project Manager and Team Manager at LSI-Logic, Synopsys, and Texas Instruments in both France and the United States.
After a stint in the academic world as a professor in high schools and universities, Catherine returned to the industry in 2018 at Menta-eFPGA, as a Field Application Engineer and managed European projects.
She rejoined Synopsys to combine both her passions - academia and industry, by establishing education and research partnerships with universities in Europe.

Abstract:

The microelectronics landscape is evolving, currently driven by AI and the adoption of the chiplets. With chips being an integral part of our daily lives, there is crucial emphasis on computing power, security, safety, and efficiency of chips.

To address the future semiconductor demand and fuel a pipeline of skilled talent, this presentation aims to discuss strategies that unite the broader microelectronics ecosystem to collaboratively address workforce development needs.

It will also focus on fostering partnerships and conducting research projects to shape the technology of the future.

Overcome electronic package design challenges

Simulation of electronic products uses mathematical models to reproduce the behaviour of a real device or circuit. Simulation software allows the modelling of circuit operation and is an essential analysis tool. Because of its highly accurate modelling capability, many companies and engineers use this type of software to teach technical programs in electronics. Simulation software engages users by integrating them into the learning experience. These types of interactions actively engage learners to analyze, synthesize, organize and evaluate content.

These solutions deepen the study of the most critical aspects of electronic product design through simulation. The focus is on the design and simulation of electronic equipment such as antennas, PCBs, integrated circuit packages or even electromechanical devices. Next we will expose industry standard solvers. These solutions help you solve any challenges involving electromagnetic phenomena, temperature, signal integrity, power integrity, parasitic magnitudes, wiring and vibration in your designs. We rely on them to achieve success in designing and simulating products such as airplanes, cars, mobile phones, laptops, wireless chargers or any other system. Over time, electronic packages have become increasingly efficient by shrinking in size, but without increasing the amount of heat dissipated during operation.

The answer to contemporary challenges is related to the complex interplay between the fields of electronic engineering (EE), mechanical engineering (ME) and materials science (MS). What may seem to be the best answer from the perspective of the electronic engineer may not necessarily be the best answer from the perspective of the mechanical engineer or the materials scientist. None of these individual answers is the best answer.

Analysis using numerical simulation software packages helps specialists in various fields to understand the functioning of packages from an electronic, mechanical and thermal point of view, as well as to understand the interaction of various parameters in different physical domains.

Moreover, we have at our disposal tools to evaluate the reliability of electronic products used in various cycles of thermal and mechanical stress (shocks, random vibrations, etc.).

Mihăilă Ioan-Alexandru, INAS SA

Văduva Radu-Andrei, INAS SA

Friday, April 26		
07:30 – 08:00	TIE$_E$, TIE$_M$ preliminary activities	Library 3rd floor hall Library, Internet Room (ground floor)
08:00 – 12:30	TIE$_E$ contest	Library 3rd floor hall
08:00 – 12:30	TIE$_E$ committee evaluation scaling	Library, Room 314 (3rd floor)
08:00 – 12:30	TIE$_M$ contest	Library, Internet Room (ground floor)
08:00 – 12:30	TIE$_M$ committee evaluation scaling	Library, Private Room (ground floor)
12:30 – 13:30	*Lunch*	*Library, Private Area (ground floor)*
13:30 – 18:00	Assessments	Library, 3rd floor hall, Internet Room
18:00 – 19:00	Steering Committee Meeting	Aula Magna
19:30– 20:30	Awarding TIE$_E$, TIE$_M$	Aula Magna
21.00	*Gala dinner*	*My Continental Hotel*

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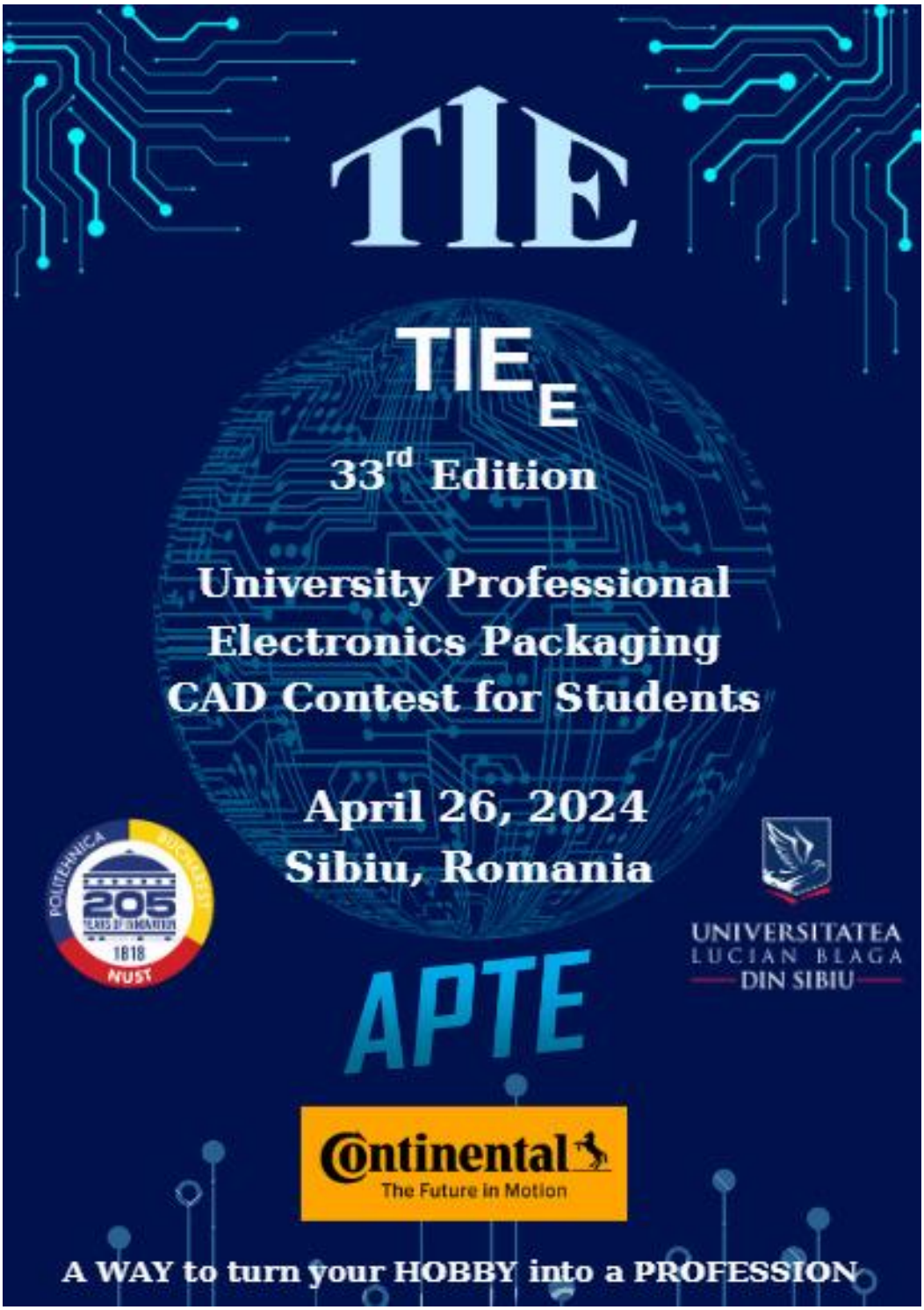
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TIE-E, A story since 1992

The TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS (TIE-E) topic represent an Electronic Packaging integrated ecosystem running in a contest environment based on the knowledge obtained during the specific curricula for each of the pillars, e.g courses for design and manufacturing of analogue, digital and mixed electronic modules, as well as on the advanced knowledge of developing PCB interconnection structures according to IPC (Association Connecting Electronics Industries) and other international standards recognized by the electronics industry worldwide. It also intends to integrate cross-discipline knowledge awareness required by real life engineering.

The TIE-E contest is a student professional contest whose objective is to promote technological computer aided design (CAE-CAD-CAM) of electronic modules. It involves designing a PCB using industry standard CAD tools during a four-hour session. The TIE-E work model well described as stage in the picture from the last stage, CAD, of the development methodology referring to how to develop sustainable product innovations by Stig Ottosson, in the 2017 book entitled "Developing Sustainable Product Innovations" that also proposed that Dynamic Product Development (DPDTM) [1]:Every year, Technical Committee (TC) is set to keep up with the latest technology and requirements for the subject development by adding new challenges year after year to the concept. The contest subject is containing in 3 consecutive parts where each part (design phase) is divided in other small tasks according to the specific design phase. Each part is evaluated, based on the evaluation table written by TC after the subject was defined.

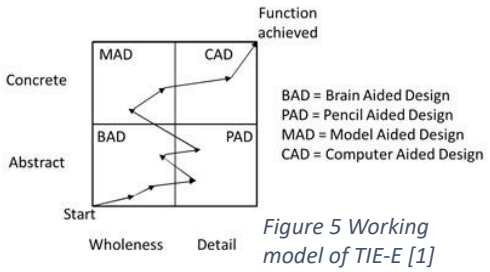

Figure 5 Working model of TIE-E [1]

1) Schematics Design & Library Creation:

This part is focused on the front-end activities from an ECAD project. Activities like project structure, page numbers, components used, rules and much more are underlined in this part. In order to get points at this part, students should pay attention to: project files and directories to be organized and renamed accordingly; component symbols to be created according to the datasheets or given schematic (terminal naming's, numbering matching etc.); schematic to be reproduced with 100% fidelity and clear manner (no overlapping items, no additional or less components, symbols or nets); page size and naming; schematic rules and correct definition of differential pairs; test point placement; DRC & Forward annotation, etc.

2) PCB Technology Definition and Block Placement Requirements

In this part, the participant shall be able to define the PCB mechanical and electrical constraints. Here the TC is verifying the project at the mechanical level by checking if the: footprints required are created according to the datasheets (including additional thermal vias); rules (ex. single ended traces/differential pair) are implemented according to the

contest requirements; PCB stack up definition; given DXF is used to define PCB outline; holes and components are placed according to the given coordinates; etc.

3) PCB Routing and Completion

This is the final step of the contest, where all previous steps are needed in order to be able to get the maximum possible points. With this final step the entire project should be finished with attention to: correct placement of the components; routing rules defined and respected; decupling capacitors used accordingly; definition of VIA numbers for the current flow or heat dissipation (Saturn PCB can be used here); definition of documentation layer; correct generation of manufacturing files: Gerber, Drill, Pick and Place, Test points and BOM; etc.

Each contestant is evaluated by a combined team formed by 2 or 3 members from industry and academia, based on an evaluation scale. This is developed by TC in collaboration with academic trainers, ensuring in the same time an clear, impartial and transparent ranking.

The proven exercise offers to the industry the chance to influence and get new candidates as follows:

- Holistic future engineers – able to start from scratch to manufacturing a complete electronic product with various potential full time job roles, as follows:
- Librarian engineers that care for integrated components CAD data up to manufacturing requirements of one's company
- The basics of electrical engineering architects able to translate requirements of new products to functional bloc diagrams
- Industry certified: SCH integrators able to translate the electronic knowledge into an electrical schematics for further usage and certified PCB designers (Layouter, Artwork designer)

TIE-E confirms that the academia's training staff's investment, in line with the expectation but also outside the normal job, it is worth all the effort, being it even voluntary!

Source: Paul Svasta, Cosmin Moisa, Norocel Codreanu, Cătălin Negrea, Mihai Cenușă "Extracurricular Environment for Electronics Packaging Knowledge Integration " 2023, 46th International Spring Seminar on Electronics Technology (ISSE), https://doi.org/10.1109/ISSE57496.2023.10168401

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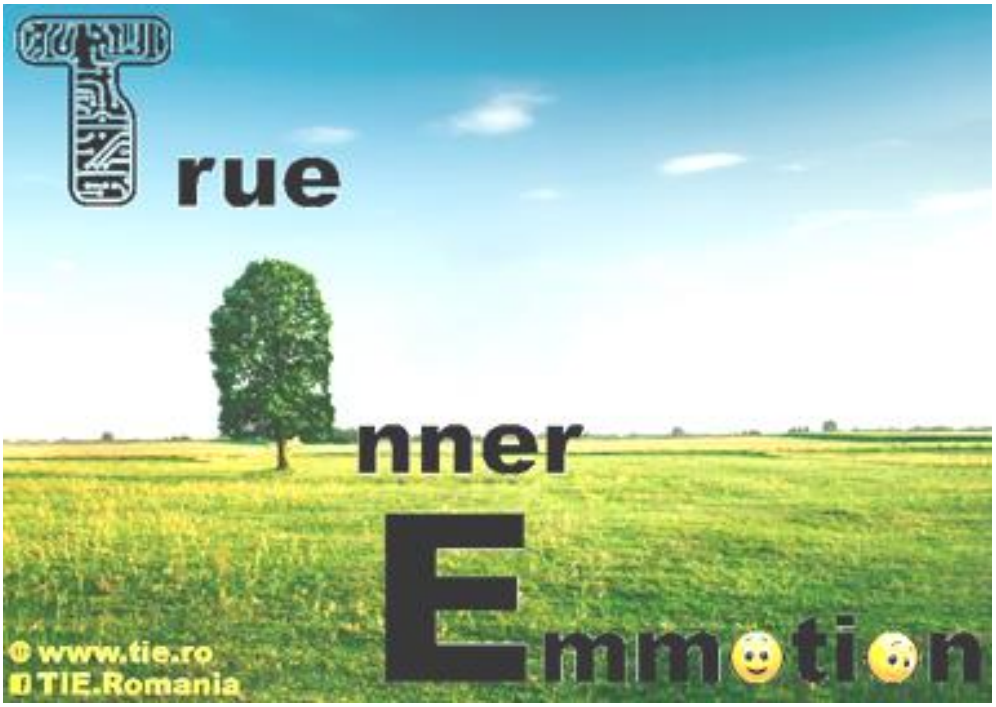

TIE Winners

Year	Name	University
2023	Vasilache Cristian	POLITEHNICA of Bucharest
2022	Ciucardel Nicolae-Marian	University of Piteşti
2021	Ioniță Alexandru	Technical University of Cluj Napoca
2020	Țurca Victor	Ştefan cel Mare University of Suceava
2019	Ghineț Dragoș	Technical University of Cluj Napoca
	Chiraș Ovidiu Marius	Ştefan cel Mare University of Suceava
2018	Goglea Alexandru Nicolae	University of Piteşti
2017	Cojocariu Gheorghe	Ştefan cel Mare University of Suceava
2016	Voina Radu	Technical University of Cluj Napoca
2015	Luchian Teodor	Ştefan cel Mare University of Suceava
2014	Grigoraş Eduard	Ştefan cel Mare University of Suceava
2013	Bostan Adrian	University Politehnica of Bucharest
2012	Aldea Alin	University of Piteşti
2011	Precup Călin	Politehnica University of Timişoara

2010	Dungă Tudor Dan	Politehnica University of Timişoara
2009	Răducanu Bogdan	University Politehnica of Bucharest
2008	Oşan Adrian	Politehnica University of Timişoara
2007	Tamaş Cosmin Andrei	University Politehnica of Bucharest
2006	Moscalu Dragoş	Gh.Asachi Technical University of Iaşi
2005	Andreiciuc Adrian	Politehnica University of Timişoara
2004	Berceanu Cristian	Politehnica University of Timişoara
2003	Munteanu George	University Politehnica of Bucharest
2002	Rangu Marius	Politehnica University of Timişoara
2001	Toma Corneliu	University Politehnica of Bucharest
2000	Vlad Andrei	University Politehnica of Bucharest
1999	Savu Mihai	University Politehnica of Bucharest
1998	Alexandrescu Dan	University Politehnica of Bucharest
1997	Gavrilaş Cristian	University Politehnica of Bucharest
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1994	Bucioc Mihai	University Politehnica of Bucharest
1993	Teodorescu Tudor	University Politehnica of Bucharest
1992	Teodorescu Tudor	University Politehnica of Bucharest

Recognition by the industry of student competences in PCB design

TIE 2024 Certificate of Competence

The „PCB Designer” certificate is awarded, after evaluation, by the TIE IC (Industrial Committee) to selected contestants, as recognition of their high level of knowledge in the field of EDA and CAD for development of electronic modules/assemblies. The evaluation is based on the worldwide known and accepted IPC standards. The certificate is offered under the “umbrella” of the Association for Promoting Electronics Technology (APTE).

Please see more details on www.apte.org.ro.

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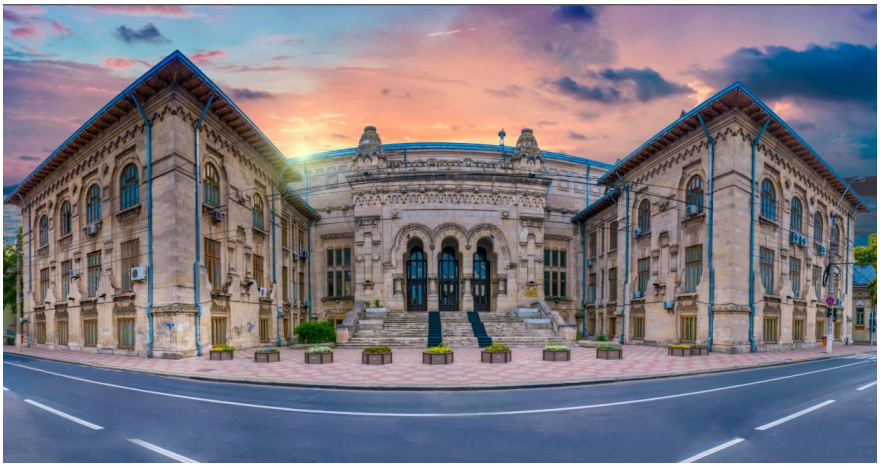

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www.tie.ro

TIE M-Mechanical

TIE M-Mechanical is a CAD Design Challenge that aims to assess students' proficiency in computer-aided design (CAD) for mechanical components, with a focus on electronic packaging and electro-mechanical assembly as shown in Figure 1. This challenge evaluates students' knowledge and skills acquired through coursework in mechanical engineering, emphasizing the design and manufacturing of mechanical components using CAD software. The challenge seeks to establish itself as a benchmark certification in the field of mechanical CAD design, particularly within the context of electronic packaging and electro-mechanical systems.

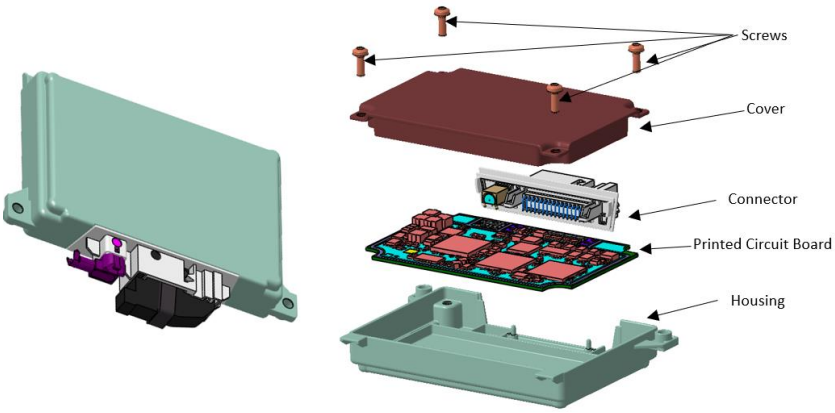


Figure 1. Electro-mechanical assembly

Objectives:

- Stimulating student's interest in mechanical engineering and CAD design, particularly in the context of electronic packaging and electro-mechanical assembly.
- Evaluating student's CAD design skills within a competitive framework, fostering a spirit of excellence and innovation in mechanical component design for electronic systems.
- Certifying student's CAD proficiency endorsed by industry experts, including the Industrial -Advisory Committee (IAC), to meet industry standards and requirements for electronic packaging and electro-mechanical assembly.
- Providing the electronics industry with a pool of skilled CAD designers ready to contribute to various electro-mechanical engineering projects, including electronic packaging solutions.
- Familiarizing students with the processes involved in designing mechanical components and assemblies for electronic packaging, ensuring compatibility with electronic modules and adherence to packaging standards.
- Cultivating a high level of professionalism in the use of CAD software systems for mechanical engineering applications in the context of electronic packaging and electro-mechanical assembly.

- Increasing awareness within the mechanical engineering and electronics industries about available talent and fostering strong partnerships between academia and industry in the realm of electro-mechanical engineering.
- Generating increased demand for mechanical engineers with CAD design skills specialized in electronic packaging and electro-mechanical assembly among current students and expanding job opportunities within the industrial sector.

Description of a subject (summary)

As a mechanical design engineer, your company won a project to create a sensor module for a well know OEM car manufacturer. To boost profits and speed up development, the company chose to use existing components (Figure 2) and make design ajustments to meet the client's needs. Modifications to the bracket and sensor ensure they fit within specified areas without altering overall functionality. The client provided a 2D drawing ("Cover.pdf") as a starting point for the cover design, which must be optimized to meet all requirements. The 3D model includes restricted areas for the new parts.

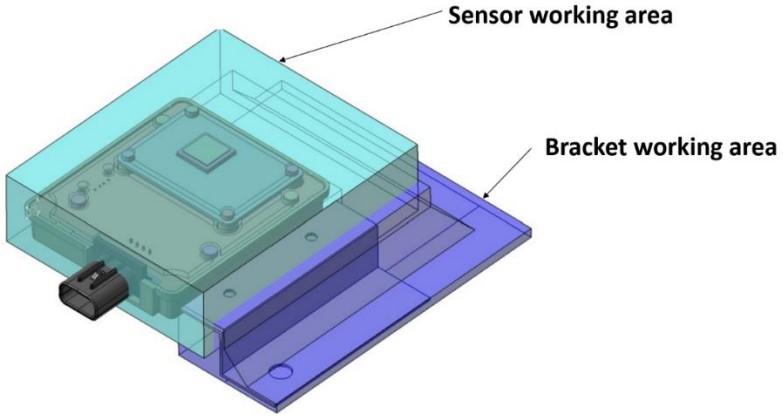
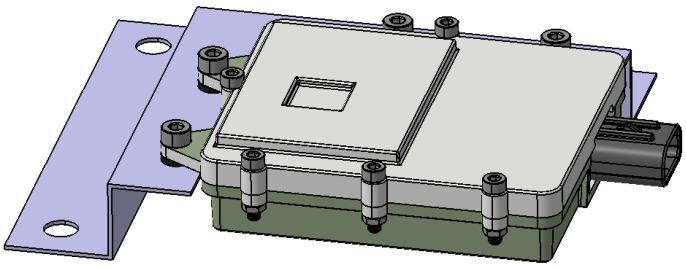


Figure 2 Existing components

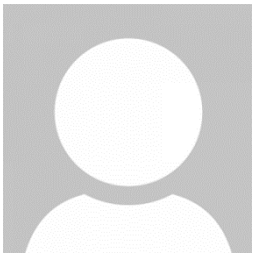
Solution



The criteria on the basis of which the student qualifies as being initiated in the evaluated topic:

- Understanding Electronic Packaging: Show knowledge of how to place electronic components and manage heat within CAD designs.
- Efficient Component Integration: Ability to seamlessly integrate electronic parts into mechanical designs while meeting industry standards.

- CAD Proficiency: Expertise in using CAD software to design, model, and simulate electronic assemblies.
- Creative Problem-Solving: Demonstrate innovative solutions to electronic packaging challenges within CAD designs.
- Detail-Oriented Design: Attention to detail in CAD designs, including precision in measurements, accurate placement of components, and consideration of assembly constraints and tolerances for electronic packaging.
- Compliance with Standards: Ensure that CAD designs meet industry standards and client requirements.
- Clear Communication: Clearly convey design intentions through CAD drawings and documentation for effective collaboration.
- Professionalism: Maintain professionalism by meeting deadlines, accepting feedback, and handling information ethically.



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***Alexandru Falk**, Continental Autonomous Mobility*

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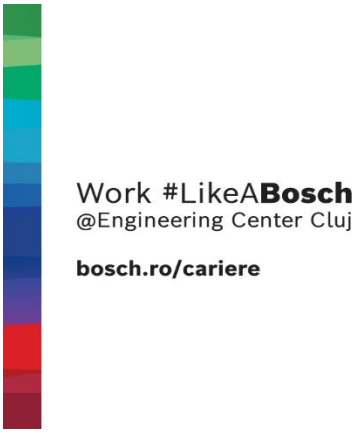
Bosch Engineering Center Cluj plays an essential role in the great transformation of the mobility sector ever since its foundation in 2013. With vast expertise in software, hardware & mechanical and reliability engineering, but also in sales planning, the Center contributes to the development of excellent products, services and innovative AI-based solutions for automated driving, connected & electric mobility. Thanks to the close collaboration with other Bosch engineering centers and with Bosch Cluj Plant, and to its state-of-the-art offices and laboratories from Cluj-Napoca, Jucu and Bucharest, the Center offers unique solutions to its clients from around the world.

Read more: https://www.bosch.ro/en/our-company/bosch-in-romania/bosch-engineering-center/



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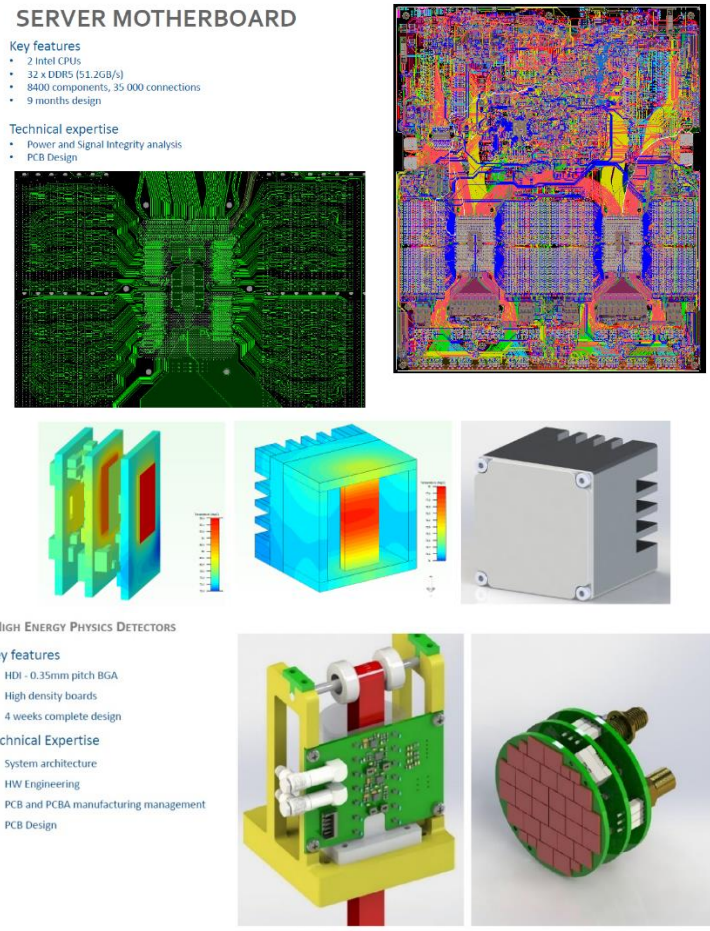
BRAINiac is one stop key provider of hardware development tools.

Brainiac Engineering

Our integrated hardware development solutions for embedded microprocessors have been widely adopted by customers worldwide in order to support the New Production Introduction (NPI), system design, hardware manufacturing & system integration.

BRAINiac is an engineering office based in Romania, Bucharest for many types of applications performed by a team of 33+ senior engineers.
The Engineering services cover areas like analog, digital, high power, nuclear and aerospace electronics, mechanical design, PCB Design, Thermal analysis, SW CAD development, Manufacturing Management, FPGA - VHDL Programming, Embedded Firmware and Product Testing.



Continental develops pioneering technologies and services for sustainable and connected mobility of people and their goods. Founded in 1871, the technology company offers safe, efficient, intelligent and affordable solutions for vehicles, machines, traffic and transportation. In 2023, Continental generated sales of €41.4 billion and currently employs around 200,000 people in 56 countries and markets.

In the time frame 1999 - 2023, Continental invested over € 2,3 billion in its Romanian operations. All three group sectors of the corporation are represented in Romania. The company has five production units and four research and development centers in the cities of Timisoara, Sibiu, Carei and Iasi. Continental has a tire distribution center in Bucharest. The company employed more than 20.300 colleagues by the end of 2023, out of which more than a third are engineers.

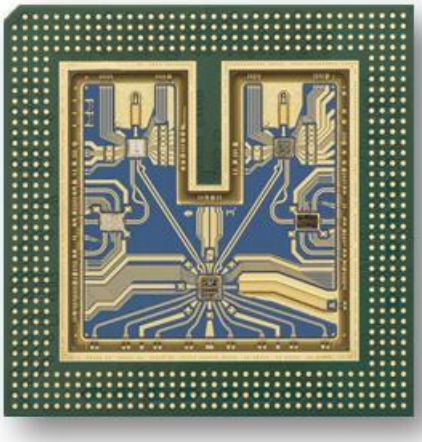
Continental Sibiu has ~4500 employees. Our location measure the size of almost 31 football fields. Location includes 6 modules of production (soon 7), 3 multi-floor R&D buildings and other amenities. You could almost feel like in a campus here…considering also that the average age in Continental Sibiu is 34.

Postal Code: 550018
Sibiu, Romania
Phone: +40 (369) 433 005
www.romania.careers-continental.com

H TEST company is a **leading supplier of test & measurement instruments and systems** for industry, education and telecommunications. We are currently operating in the **Czech republic, Slovakia, Austria, Hungary and Romania**.

We are providing test and measurement solution to the industry

- **Oscilloscopes**
- **Spectrum & signal analyzers**
- **Vector network analyzers**
- **Signal sources**
- **Component & material measurements**
- **General purpose test instruments**
- **Power supplies**



Our core value:

- **Technical strenght and depth**
- **Technical consultancy and market knowledge > 25 years experience**
- **Application and solution focus**
- **Creating value for our customers**

H TEST ROMANIA SRL
B-dul Cetății nr. 5-7-9
300389 Timișoara, Romania

www.htest.ro

ICCO® EMT
Enjoy your business!

500460 Brasov, Romania
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Fax +40 268 401 240
emt@icco.ro
https://www.icco.ro/en/emt

ICCO EMT established in 1997, as partner for producers in the semiconductor and electronics industry, offering specialized equipment and services. Over the years, the company collected experience in implementing sophisticated equipment necessary for semiconductor and electronic production processes. We set up and supply solutions for turn-key electronic production and complete production lines. **ICCO EMT** offers contract manufacturing services both for small volumes (NPI) and for products in large series.

Due to the high diversity of the products we offer to our customers, we are now able to configure and provide turn-key solutions for electronic production, fully functional manufacturing lines.




Kulicke & Soffa (NASDAQ: KLIC) is a leading provider of semiconductor and electronics assembly solutions serving the global automotive, communications, computing, industrial markets, and consumer.

Kulicke & Soffa
Technology . Innovation . Solutions

BTU

amx
WWW.AMX-AUTOMATRIX.COM

NUTEK®
PCB HANDLING & TRACEABILITY
CLEVER AS EVER

OMRON

KROSCHU KROMBERG & SCHUBERT

With a global presence of more than 50,000 employees in over 50 locations, Kromberg & Schubert is among the worldwide leading suppliers of wire harness systems, cables and injection moulding technologies.

Our vision is to...

...shape the future of mobility on the global stage as an internationally respected specialist for wiring systems. With innovative wiring systems by Kromberg & Schubert that accompany our customers from the automotive industry into a sustainable and mobile future.

We are present in Romania with Competence Centers and Production Facilities in: **Sibiu**, Medias,Timisoara, Nadab.

PRODUCTION OF COMPLEX WIRE HARNESS SYSTEMS

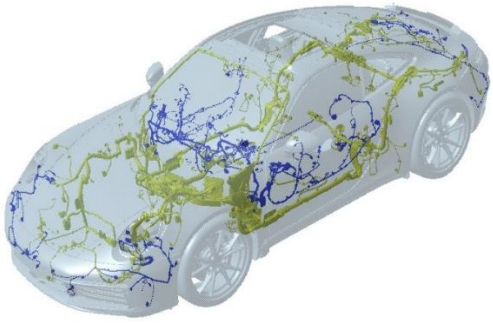
Our product portfolio covers customer-specific wire harness systems as well as sub-assemblies for ABS, headlamps, doors, seats, air-conditioning and high-voltage applications.

PLASTICS ENGINEERING

The entire competence from a single source: Design & development of plastic parts and injection moulding tools, as well as the validation, integration, and production of serial parts from one competitive injection moulding supplier.

RESEARCH AND DEVELOPMENT

Innovative topologies for Electrical Systems and architectures for future signal and power transmissions. Optimised product development processes including dimensioning, benchmarking and in-house validation capabilities.



THE SPECIALIST FOR ELECTRICAL DISTRIBUTION SYSTEMS

Building the Future of Data Infrastructure

Marvell Technology, Inc. (NASDAQ: MRVL) develops and delivers semiconductor solutions that move, store, process and secure the world's data. As a trusted leader in essential data infrastructure semiconductor technology, Marvell's cloud-optimized silicon powers innovation in cloud and AI, carrier infrastructure, automotive and enterprise networking markets. With a comprehensive portfolio of electro-optic, Ethernet, processor, security and storage products and IP, the company offers merchant, semi-custom and fully custom options to address a range of customer requirements.

Data Center

Cloud-optimized silicon for driving scalable AI platforms.

Carrier

Industry-leading RAN and Cloud-optimized 5G Silicon

Automotive

End-to-end networks for the **software-defined** vehicle

Enterprise

Intelligent networking for the borderless enterprise

- Fabless semiconductor company
- Innovating since 1995
- 10,000+ patents worldwide
- Headquartered in Santa Clara, California
- Research and development centers located in USA, Israel, India, Vietnam, Argentina, Italy, Canada, Germany, and China
- Focused on excellence in Engineering with 85% of employees in technical roles

To learn more, please visit us at www.marvell.com.
Scan the QR code to view the Marvell 101 video.

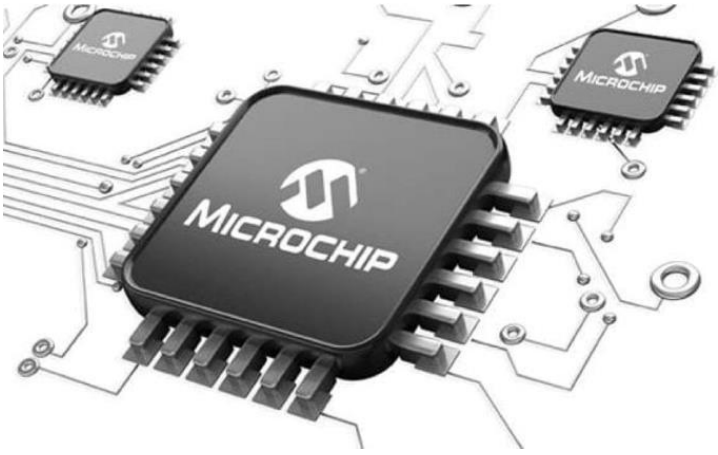
Microchip Technology Inc.

Microchip Technology is a leading provider of smart, connected and secure embedded control solutions. As a global company with over 22,000 employees, Microchip has a robust presence in Romania. Our company has an extensive portfolio that includes advanced **microcontrollers, digital signal controllers, microprocessors, mixed-signal, analog, interface, and security solutions**, alongside cutting-edge **FPGA, connectivity, memories, and power management semiconductors**. Our innovative solutions empower a diverse clientele, serving approximately **125,000 customers** across key sectors such as **industrial, automotive, consumer, aerospace and defense, communications, and computing**.

Romania Design Center (RDC) – A Hub of Technological Excellence

At the heart of our innovation lies the **Romania Design Center (RDC)**, a crucible of talent and expertise accommodating over **multiple business units**. The RDC is instrumental in the **development of analog, digital, and mixed-signal products**, encompassing all stages from design and verification to validation. Furthermore, it is a nucleus for **software development, field technical customer support**, and the design and application development of **8-, 16-, and 32-bit microcontrollers and microprocessors**.

Strategically located in the **AFI Business Park,** adjacent to the Electronics, Telecommunications and Information Technology (ETTI), the RDC is not just a workplace but a nurturing ground for budding engineers. This initiative is a testament to our commitment to nurturing talent, with many interns seamlessly transitioning to full-time roles, thereby fostering long-term professional growth. We are dedicated to mentoring our interns and employees, guiding them towards achieving their fullest potential.



As a world leader in secure connectivity solutions for embedded applications, NXP Semiconductors is pushing boundaries in the automotive, industrial & internet of things (IoT), mobile, and communication infrastructure markets while delivering solutions that advance a more sustainable future.

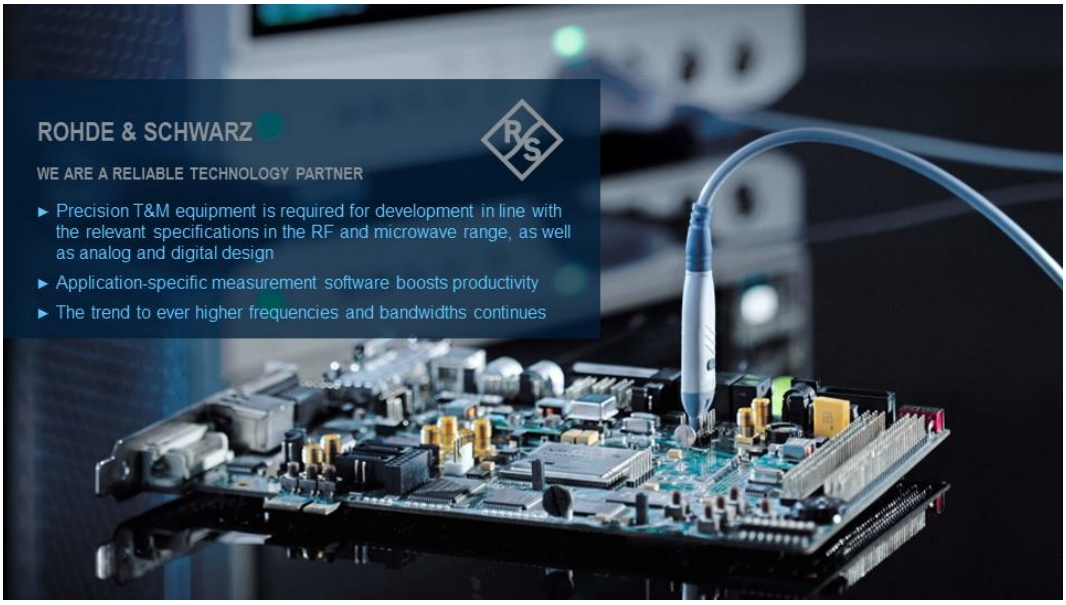
The company has had substantial growth over the last few years, with currently 1050 team members at NXP Romania in Bucharest. In May 2023, the company opened its second research and development (R&D) center in Sibiu and it continues to recruit, having open positions in all key areas of development.

NXP Romania contributes to the development of solutions for automotive, consumer and industrial IoT markets by developing software platforms that integrate NXP components and software from partners. In addition to software development, NXP also invests in research as part of intellectual property creation programs.

The R&D centers of excellence have more than 20 years of experience in designing, developing and innovating software products. The center of excellence in Bucharest focuses on two areas in continuous transformation: automotive and IoT. As automotive architectures are evolving, the teams are specialized in developing integrated software products that enhance customer experience by providing reference hardware and software platforms that are easy to use and configure. NXP also has dedicated teams that focus on IT service management and chip sales and order management operations.

As a world leader in secure connectivity solutions for embedded applications, NXP Semiconductors is pushing boundaries in the automotive, industrial & internet of things (IoT), mobile, and communication infrastructure markets while delivering solutions that advance a more sustainable future.

Each year, NXP Romania hosts interns who learn the specifics of software development in Automotive, Edge Computing and IoT. We are proud that our interns extend their experience with practical contributions in real-life projects. Search for latest internship openings on https://shorturl.at/hkluP



Rohde & Schwarz is a global technology group striving for a safer and connected world. With its Test & Measurement, Technology Systems and Networks & Cybersecurity Divisions, the company creates tomorrow's innovations today. The company's leading-edge products and solutions empower industrial, regulatory and military customers to attain technological and digital sovereignty.

Innovation has been part of Rohde & Schwarz since the very beginning. The company founders Dr. Lothar Rohde und Dr. Hermann Schwarz were technological pioneers. With their hands-on entrepreneurial spirit, the two college friends entered the unexplored field of RF engineering. Ninety years later, the company is still pushing technological boundaries – as a successful shaper of cutting-edge technologies such as artificial intelligence (AI), 6G, cloud and quantum technologies.

The privately owned company is known for stability and resilience. Independence is at the core of its entrepreneurial identity. The company finances its growth with its own resources. Because the company does not have to think in terms of quarterly results, it can plan sustainably for the long term. The high added value of Rohde & Schwarz makes the company a reliable, trustworthy and relevant partner for its customers.

TEST & MEASUREMENT	**TECHNOLOGY SYSTEMS**	**NETWORKS & CYBERSECURITY**
Wireless I Industry, Components & Research I Aerospace & Defense Testing I Automotive	Secure Communications I Critical Infrastructure & Networks I Government I IP Network Analytics I Broadcast, Amplifiers & Media	Endpoint Security I Secure Networks I Certified & High-Grade Crypto Solutions

Keytek Innovation is a design house capable of ensuring the development, security, and efficiency of custom electronic systems from idea to production, regardless of any challenges that may arise during the process. Our analytical skills and critical thinking, combined with a solid background in electronic engineering and hardware system design, will help you reduce time-to-market while keeping the development process cost-effective.

At Keytek, we boast extensive experience in High-Density Interconnect (HDI) PCB design, and we utilize cutting-edge 3D Electromagnetic (EM) analysis software and circuit simulation tools to perform signal and power integrity analysis. We understand the importance of this in today's digital world, where new standards require higher data rates, faster speeds, and increasingly complex designs. To shorten the debugging time, ensure product performance, and preemptively address future issues, our design process includes a comprehensive suite of analysis and verification techniques. Ensuring consistency, repeatability, and reproducibility are our primary objectives when validating and verifying various systems. To guarantee the success of these processes, we utilize measurement instruments from industry-leading companies and post-process the results using various programming languages specifically designed to streamline the validation and verification steps.

Optimal Designs is an established high-frequency design and simulation software supplier catering to North American and European clients. As an established collaborator of Dassault Systèmes for CST Studio Suite, we specialize in providing state-of-the-art solutions customized to meet the ever-changing requirements of the high-speed PCB design industry. We have extensive knowledge and experience in various areas of design and simulation, such as GBit channel design, signal and power integrity, EMI/EMC government qualification, and electromagnetic-coupled thermal management.

Our experienced staff excels at developing advanced 3D passive component designs, providing cutting-edge solutions in PCB and coaxial connectors, power divider networks, 2D/3D filter design, and antenna design. Our team is capable of addressing complex design scenarios, whether it involves creating designs for advanced communication systems or assuring the dependability of crucial electrical components. We prioritize achieving optimal performance, reliability, and adherence to all applicable requirements. Optimal Designs is committed to pushing the limits of achievable goals, utilizing our extensive industry expertise and technical skills to help our clients maintain a competitive edge in the ever-changing field of high-speed design and simulation.

Net Digital Service produce sabloane SMT de inalta calitate si precizie, prin taiere cu laser. In acest moment aceasta metoda de taiere este cea mai raspandita, intrucat are avantajul obtinerii unei precizii ridicate a sabloanelor si a unei forme imbunatatite a peretilor aperturii, care permite o depozitare optima a pastei de lipit pe pcb-uri. NDS are in dotare masini de taiat cu laser LPKF, considerate a fi cele mai precise si fiabile masini de acest tip de pe piata. Sabloanele SMT sunt de mai multe tipuri, in functie de sistemul de prindere/tensionare. Sabloanele pot fi autotensionate (lipite pe o panza tensionata intr-un cadru de aluminiu – „mesh-glued"), sau pot folosi rame de tensionare pneumatice. Exista o multitudine de rame de tensionare pe piata, dintre care cele mai des utilizate sunt ramele VectorGuard, Alpha Tetra si Zelflex. Pe langa toate aceste tipuri de sabloane, NDS ofera ministenciluri, sabloane autotensionate (mesh-glued), tratament nanocoating, sabloane in trepte (step-stencils) etc. Pana la sfarsitul lunii iunie 2024, va fi disponibil si tratamentul prin electrolustruire (electropolish) a sabloanelor. NDS este certificata ISO 9001. Toate sabloanele produse sunt controlate cu sistemul ScanStencil, astfel incat erorile de taiere sunt eliminate in intregime.

Livrare 24-48 de ore, oriunde in Romania si Europa.

NET DIGITAL SERVICE S.R.L.

Parc Industrial Borş, nr.2/D, Borş 417075, jud. Bihor, România

Tel. 0359.192.819 - office@nds-service.com - www.nds-service.com

Parteneri Dassault Systèmes

Caelynx Europe este unic distribuitor autorizat al produselor Dassault Systèmes's SIMULIA in Romania si Bulgaria:

- **CST -** simulare Electromagnetica
- **ABAQUS -** unul din produsele de baza din portofoliul SIMULIA, este recunoscut ca fiind unul dintre cele mai avansate softuri de analiza cu elemente finite.
- **Isight** - solutie de automatizare si optimizare a simularii de produs
- **Tosca** -solutie de optimizare a produsului
- **FE Safe-** solutie calcul de oboseala si durabilitate
- **3D Experience**

Centru autorizat de formare.

MAC`s MEDICAL Group ofera solutii medicale spitalelor si in special disciplinelor chirurgicale, in Europa centrală si Europa de SE, având sediul central în Viena. Suntem în mod special mândrii de faptul că, din pionieri ne-am transformat în furnizor de top al implanturilor cardiovasculare. Astăzi, 20 de ani mai târziu suntem din nou din poziţia de pionieri în medicina regenerativă şi chirurgia minim invaziva. De la fondarea noastra, ca afacere de famile, in 1995 pana astazi, ne-am ghidat si ne construim in viitorul prin valorile: Calitate, Eternitate, Rezultate pe termen lung, Comunicare si nu in ultimul rand Libertate.

Calitate: Acumulam experienta medicală profesională din 1984, în special în sistemul circulator – unde am învățat, „calitate" nu este doar un cuvânt. Am înțeles că o îmbunătățire a calității de doar 1% ar putea însemna 100% pentru un pacient.

Eternitate: Foarte curând, am aflat că doar un model „win-win" funcționează si poate dainui in eternitate! Pentru noi este normal și important să ne pese de preocupările partenerilor noștri și noi numim aceasta:

Rezultate pe termen lung: Am invatat că o dezvoltare continuă este posibilă doar prin impartasirea experienței cu partenerii noștri (clienți și furnizori). Drept urmare, ne străduim sa dezvoltam relații pe termen lung și sa cultivam o cooperare deschisă și constructiva prin:

Comunicare: Echipa MACs MEDICAL comunică in toate nivelurile, deoarece credem că doar o echipă coordonată este capabilă să răspundă nevoilor partenerilor noștri. Pentru a dezvolta în continuare o echipă profesionistă are nevoie de:

Libertate: Noi, MAC's MEDICAL Group, muncim din greu pentru a combina toate aceste valori. Admitem că nu este simplu și cu siguranță nu este ușor. Dar, scopul nostru este să oferim un serviciu de înaltă calitate și nu „easy going story"!

MAC's MEDICAL Group
Your Partner with Heart

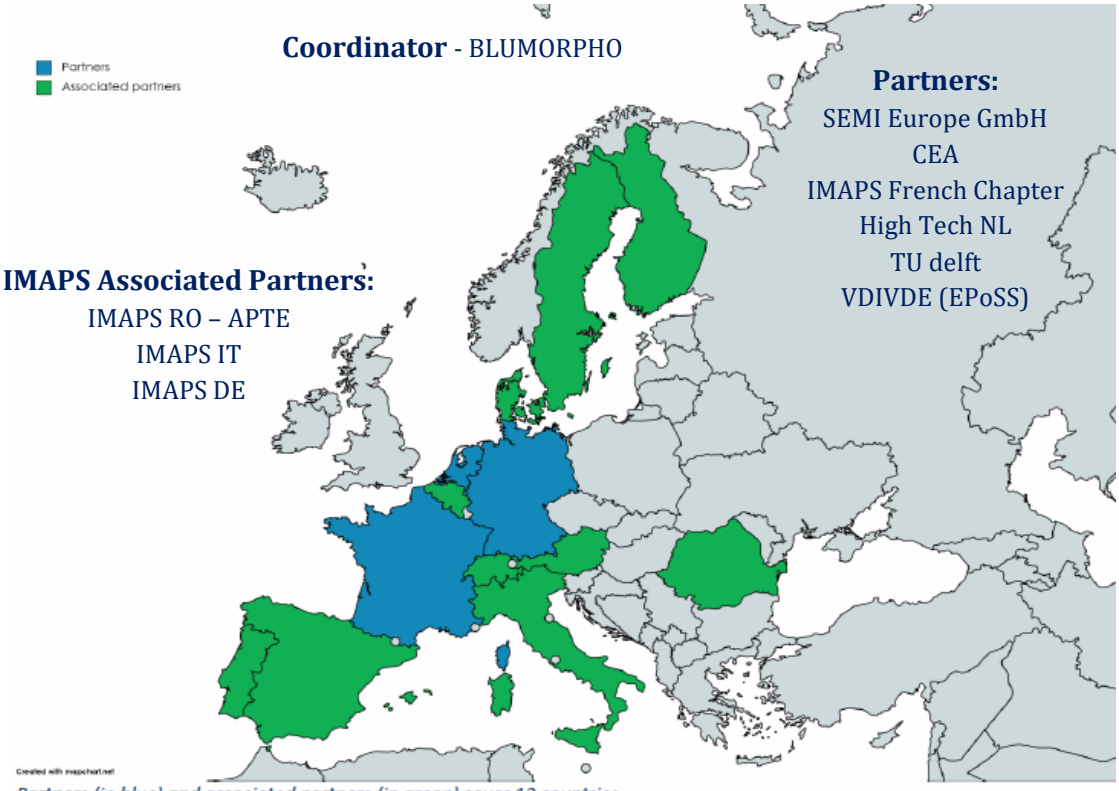
KDT JU
Key Digital Technologies Joint Undertaking

PACK4EU

PACK4EU Project
BOOSTER PACKAGING FOR EUROPE

PACK4EU Project has **two main objectives**, the "Creation of the Pan-European network" and as the second one to "give guidance" to the policy makers of the trilogue, European Council, Member States (MS), the Parliament, who ask what to do for the entire value chain.

PACK4EU Partners and Associated Partners



Partners (in blue) and associated partners (in green) cover 12 countries

Contact details:

Bogdan MIHĂILESCU – bogdan.mihailescu@apte.org.ro

Flamenco

Forward Looking Approaches for Green Mobility Ecosystem Network Collaboration

About the Project

Project FLAMENCO is an ERASMUS+ Co-funded project with the main goal to analyse and pilot forward-looking approaches and methods to enable and make sustainable collaboration on the skills intelligence in the Automotive-Mobility Ecosystem.

The Purpose

The purpose of the Flamenco project is to make the collaboration of the existing partnership pragmatic and sustainable (outreach to other Pact for Skills partnerships as a good practice) so that it brings valuable information about new technological and societal trends, related skills needs training offer/needs and other goals in terms of the skills intelligence leading up to the re-/up-skilling within the European mobility ecosystem.

Activities

The project's main activities will be to analyse the sector in cooperation with stakeholders in terms of the needs, tools, requirements and goals of the sectoral collaboration on skills intelligence via different methods, such as

- desk research
- surveys or workshops
- identification of collaboration models
- development of unified methodology and approach

The project will produce recommendations and good practices in the form of case studies and will provide them alongside the tested, frequently updated and validated methods which are to be rolled-out in different Pact for Skills partnerships and sustained after the project ends.

acea · APTE · Automotive Skills Alliance · educam · EUIO SPI · ISCN · InterTradeCard · Olife · Transilvania IT · TU Graz · VSB Technical University of Ostrava (Project coordinator)

Co-funded by the European Union

Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the European Education and Culture Executive Agency (EACEA). Neither the European Union nor EACEA can be held responsible for them.

www.project-flamenco.eu

WE HUB for digital transformation

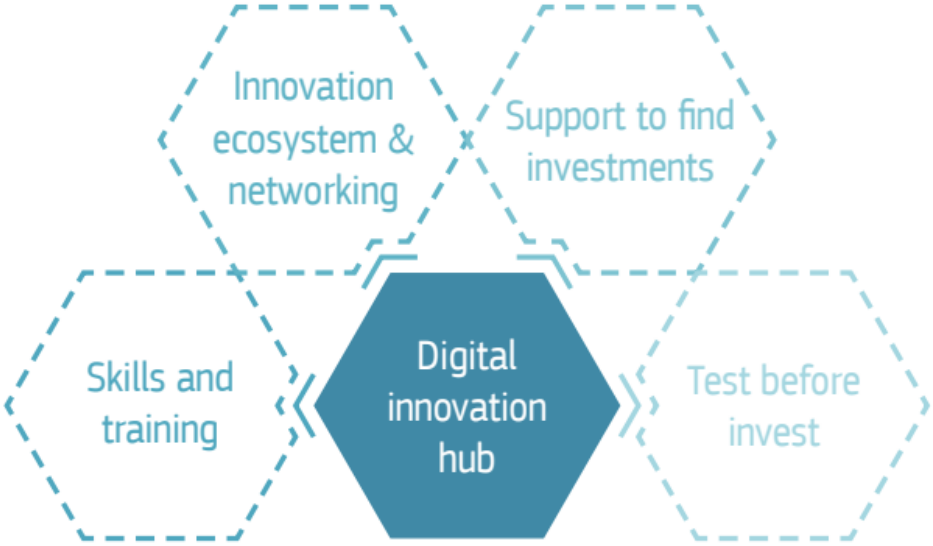
Co-funded by the European Union

EDIH European Digital Innovation Hubs Network

Wallachia eHUB

Drive innovation and digitalisation to growth

Free services offered by Wallachia eHUB for companies



WE HUB for digital transformation

Project Coordinator:

USH PRO BUSINESS

Danube Engineering Hub

TEC TECHNOLOGY ENABLED CONSTRUCTION

APTE ELINCLUB

ub UNBOX management solutions

audit business consulting

BUCHAREST PROMOROBOTS

KFactory

HEVECO

OMEGA TRUST

PETAL oil & gas equipment

integrisoft

Greentronics

Beia CONSULT INTERNATIONAL

InPULSE CONSULTING PARTNERS

Contact details:

Bogdan MIHĂILESCU – bogdan.mihailescu@apte.org.ro
WeH's profile – www.wallachiaehub.ro

ELINCLUS ELectronic INnovation CLUSter

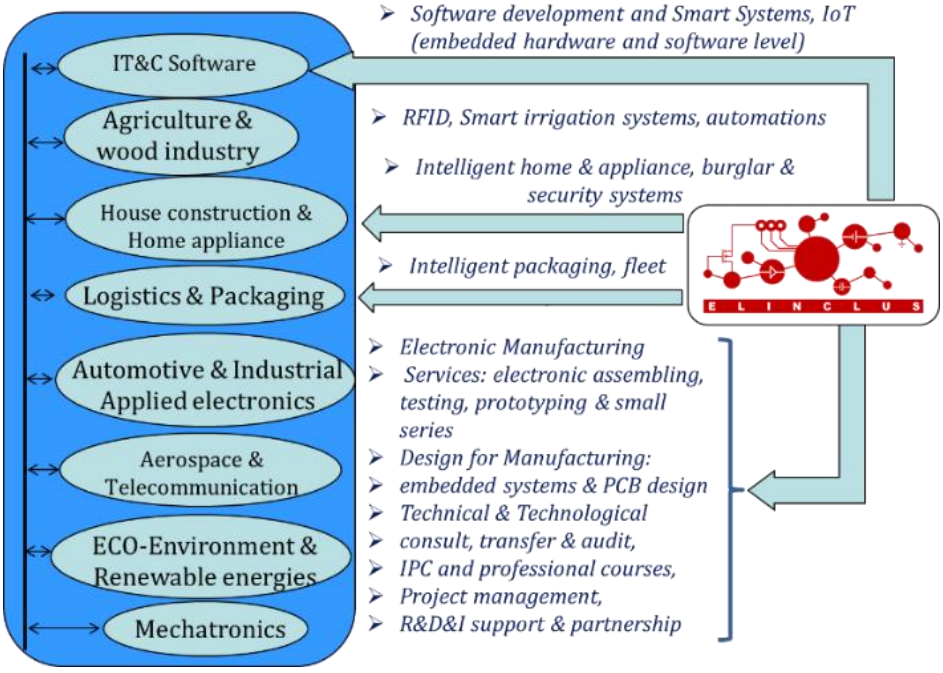
EMC: Association for Promoting Electronics Technology – APTE (www.apte.org.ro)

Founded 2011; 94 registered members

President: Prof. DHC. mult. Paul SVASTA,Ph.D.

Executive Manager: Lect. Eng. Bogdan Mihăilescu, Ph.D.

- Founding member of the Clusters Association from Romania, CLUSTERO - www.clustero.eu
- European Cluster Excellence Initiative Silver Label Certificate from ESCA since 2016
- Founding member of the IT Cluster Network from Romania comprised of 9 members 9: Transilvania IT Cluster, ALT – Brașov, Banat Software, Innovative Clsuter Open Hub, INOMAR, **ELINCLUS**, ICT Oltenia, ICT Cluster Lower Danube și Smart Alliance Cluster.
- Founding member of the regional Digital Innovation Hub – Smart e-Hub https://smartehub.eu/



• **E-mail**: office@elinclus.ro **Web page**: **www.elinclus.ro**

ASSOCIATION FOR PROMOTING ELECTRONICS TECHNOLOGY (ASOCIAȚIA PENTRU PROMOVAREA TEHNOLOGIEI ELECTRONICE)

IMAPS ROMANIA

A globally-competitive workforce with theoretical, as well as applied engineering/hands-on, education must be trained. In addition to the areas of science, engineering, microelectronics, and packaging, this training must encompass the broader areas of business, economics, ethics, foreign culture, and languages.

The Association for Promoting Electronics Technology (APTE, see https://apte.org.ro/) is IMAPS Romania. APTE was founded in 2002, by the Center for Technological Electronics and Interconnection Techniques (UPB-CETTI) together with highly respected members of the electronics industry, in order to support the electronics packaging education and engineering, in a climate of trust, ethics, and social responsibility.

APTE/IMAPS Romania is the management entity of the ELINCLUS Cluster (see http://elinclus.ro/), which has currently 94 members. ELINCLUS was established starting from the economic relationship existing between UPB-CETTI (which developed a Technological and Business Incubator, entity accredited by the National Innovation and Technology Transfer Network – ReNITT) and companies from Bucharest and Ilfov county. This structure has offered to ELINCLUS the status of a regional cluster in the field of electronics.

APTE offers annually a comprehensive set of short courses and training classes in the area of electronics packaging, IPC standards certification, management, and industrial development, in order to serve the needs of the electronics industry. APTE organises annually The International Symposium for Design and Technology in Electronics Packaging (SIITME, see http://siitme.ro/) and the Interconnection Techniques in Electronics (TIE, see www.tie.ro/) Professional Student Design Contest.

Contact:

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023496 - Bucharest, Romania
Phone: +40213169633
E-mail: apte@apte.org.ro

ITEC Information Technology in Electronics Research Center

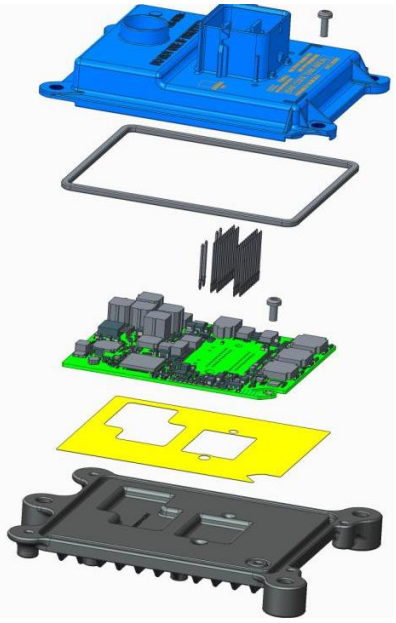
TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

ITEC Research Center

belongs to the Technical University of Cluj-Napoca having 25 researchers in Embedded Systems (electronics & software). ITEC can access the entire infrastructure of Technical University of Cluj-Napoca, resources from all other research centers and resources from Romanian University Alliance.

ITEC Competencies

- Circuit design: modeling, simulation and cross-simulation of electronic circuits (analog, digital, power, RF/EMI) & system design: modeling and simulation for electro-mechanical systems: power devices, actuators, mechatronics;
- HW Application design: fast-prototype design, PCB design for mass production, BOM/AVL design, DfM & DfT for embedded applications, power supplies, interface/signal conditioning boards;
- SW Application design: embedded control applications for OS and non-OS targets;
- TW Application design: testing and design of testing systems: SW and HW testing process, HiL and SiL, design of test-cases for SW;
- Training services: LabVIEW trainings, Embedded Systems trainings, TW and HiL operation;
- PCB DESIGN: DfX, SI and PI.



Contact

Information Technology in Electronics Research Center | Technical University of Cluj-Napoca 400027, G. Baritiu 26-28, Cluj-Napoca, Romania | E-Mail: gabriel.chindris@ael.utcluj.ro

BRAȘOV WELCOMES TIE 2025

TIE 2025

TIE$_E$, TIE$_M$, TIE$_{Eplus}$, TIE$_{Mplus}$, TIE$_{Tplus}$, TIE$_\mu$

April 2 – 5, 2025

In the spring of 2025, April 2-5, Brașov will be honored to host the traditional student competition: the 34th edition on **Technologies of Interconnection in Electronics**, an Electronics Packaging Specialized Event, ***TIE***, with its related contests (***TIE$_E$***, ***TIE$_M$***, ***TIE$_{Eplus}$***, ***TIE$_{Mplus}$***, ***TIE$_{Tplus}$***, ***TIE$_\mu$***).

Old Town and Tâmpa Peak (*alt. 960m*), photo source

Brașov is a medieval city, founded in the XIII century, where nature, history, and modern times blend. The city features the first school in Romania. Academically, the Transilvania University of Brașov is the largest university in central Romania, with over 75 years of tradition.

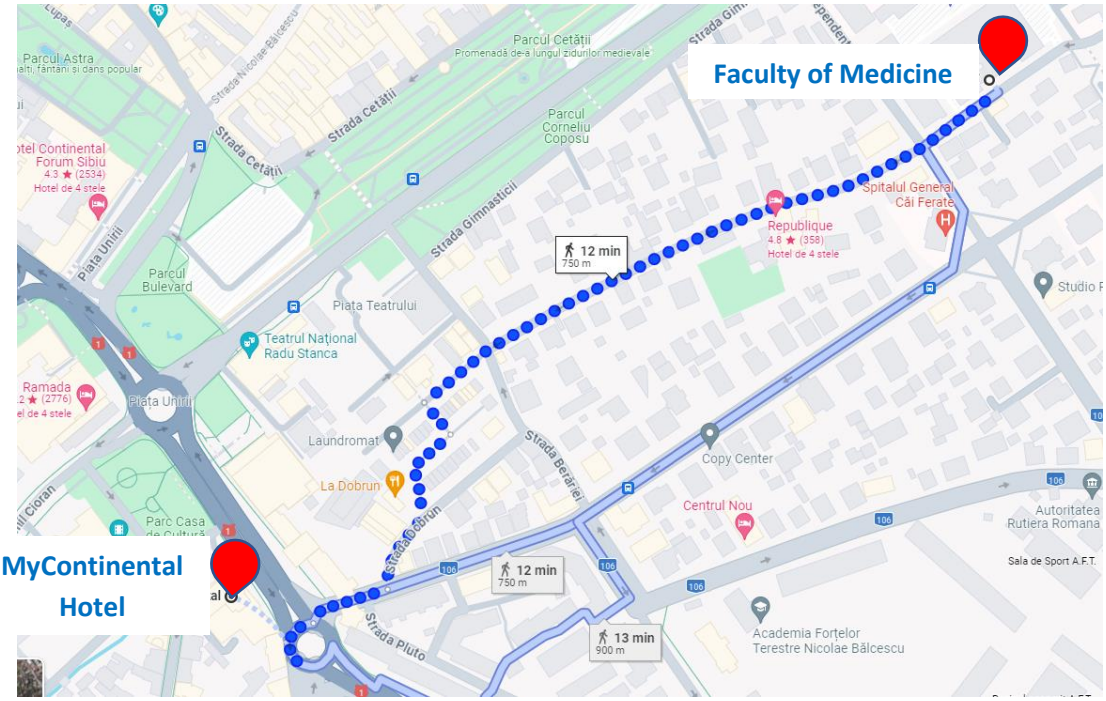
Brașov has a significant industry also related to electronic design, mainly in the automotive area, with activities ranging from manufacturing automotive parts to embedded systems design and programming. Another common field in the local industry is consumer electronics, featuring both design and development.

Transilvania University of Brașov and ***Center Regional Development Agency*** are looking forward to meeting you in Brașov!

Titus BĂLAN, PhD
Dean of the Faculty of Electrical Engineering and Computer Science, Brașov

Venue of the TIE 2024

The TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS 2024 contest event will take place at the **ULBS Library** from **Faculty of Medicine**, Lucian Blaga Street 2A, Sibiu.




Continental
MICROCHIP
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