TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

POLITEHNICA BUCHAREST 1818

APTE Association for Promoting Electronics Technology

TIE

TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry - wide Student Challenges

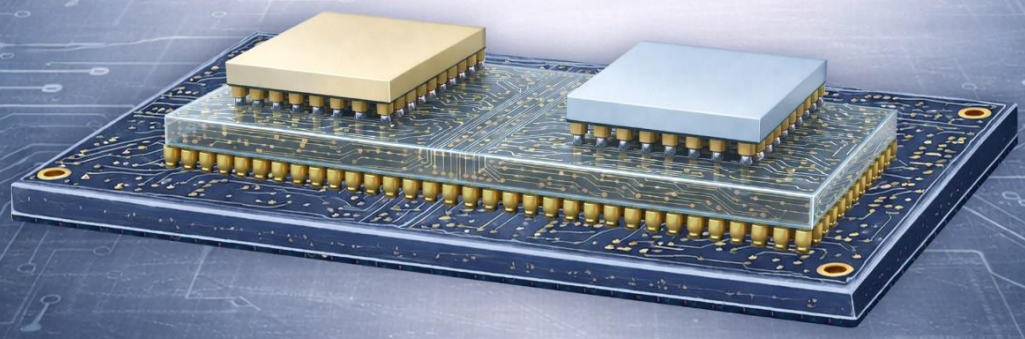
A WAY to turn your HOBBY into PROFESSION

INTERNATIONAL EDUCATION PLATFORM FOR STUDENTS AND TALENTS IN ELECTRONICS PACKAGING

22nd - 25th April 2026 • Cluj-Napoca, Romania

TIE Challenges:

- **TIE-E** PCB Design Challenge
- **TIE-E+** Signal & Power Integrity Challenge
- **TIE-M** Mechanical CAD of the Electronic Systems Challenge
- **TIE-M+** Structural Analysis of the Electronic Systems Challenge
- **TIE-T+** Electrical System Thermal Management Challenge
- **TIE-μ** Advanced Package Design and Simulation Challenge
- **TIE-n** Chip Implementation Challenge



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TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry-wide Student Challenges

A WAY to turn your HOBBY into PROFESSION

TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS

INDUSTRY-WIDE STUDENT CHALLENGES

35th Edition

Technical University of Cluj-Napoca,

April, 22 – 25, 2026

TECHNOLOGIES OF INTERCONNECTIONS IN ELECTRONICS – 2026
INDUSTRY-WIDE STUDENT CHALLENGES
Program Brochure

Welcomes to TIE 2026 Event

Dear participants at the 35th TIE edition,

Cluj-Napoca, Romania

TIE 2026 marks a new milestone for the international education platform dedicated to students and emerging talents in electronic packaging. Built on a long tradition of connecting academia, industry, and young talents, TIE continues to serve as a gateway for the next generation of specialists who will shape the future of microelectronics and advanced manufacturing.

This year, the platform expands its horizon with a stronger focus on advanced electronic packaging—covering cutting-edge topics such as heterogeneous integration, system-in-package architectures, power electronics packaging and high-density interconnect technologies. These additions reflect the rapid evolution of the global semiconductor ecosystem and the growing need for multidisciplinary expertise.

Dear students: TIE 2026 is your moment to step into the future of electronic packaging.

Here, students and young talents from several countries come together to explore ideas, challenge themselves, and discover what they are truly capable of achieving.

As an international education platform, TIE has always been a place where passion meets opportunity — where theory becomes practice, and where curiosity becomes innovation. This year, the journey grows even more exciting. TIE expands into the frontier of advanced electronic packaging, opening the door to topics that define the next era of technology: heterogeneous integration, system-in-package design, thermal management, structural analysis, electronics packaging, and high-density interconnects.

The Technical University of Cluj-Napoca becomes your campus, your laboratory, and your launchpad.

You'll learn from experts, collaborate with peers, build real solutions, and experience the thrill of turning knowledge into impact. Whether you dream of designing the next generation of chips, solving complex engineering challenges, or shaping the technologies that will power tomorrow, TIE 2026 is the place where those dreams begin to take form.. And please don't forget: TIE 2026 represents the "situ" here your talent meets its future.

We are delighted to welcome participants to Cluj-Napoca, where TIE 2026 will bring together students, researchers, and industry leaders and experts for an inspiring program of workshops, competitions, demonstrations, and knowledge exchange. Together, we

continue to build a vibrant community that supports learning, innovation, and excellence in electronic packaging.

We wish all participants a pleasant and productive stay in **Cluj Napoca, Romania!**

Prof. D.H.C. mult. Paul SVASTA, Ph.D.
IEEE Fellow
National University of Science and Technology
POLITEHNICA of Bucharest, Romania
APTE-Association for Promoting Electronics Technology
TIE General Chair

Prof. Ovidiu POP, Ph.D.
Technical University of Cluj-Napoca
Dean of Faculty of Electronics, Telecommunications and Information Technology
TIE General Co-Chair

35 Years of TIE – Building Talent for the Future of Electronics in Romania

Congratulations on the 35th edition of TIE! Driven by real industry needs and practical applicability, TIE continues to evolve. This year marks an important milestone with the launch of a new vertical – TIE-n (Nano): the Chip Implementation Challenge – complementing the existing two non-electrical and four electrical verticals that have consistently strengthened Romania's electronics value chain with well-prepared talent.

Beyond formal Bachelor and Master programs, extracurricular initiatives such as TIE play a decisive role in developing strong competencies and shaping valuable engineers. TIE is not just a competition, but a complete learning journey: from industry-inspired problem definition and student training, to hands-on project work, academic mentoring, and a final public presentation evaluated by professors and industry experts. It is a joint effort, built shoulder by shoulder by students and professors.

As Romania's microelectronics industry accelerates thanks to projects as IPCEI or Chips JU, such learning models become essential for reskilling and upskilling the workforce. This growing relevance underscores the importance of sustainable support for applied education, which is why an IPCEI workshop was organized under TIE 2026—bringing together industry, universities, and decision-makers from public administration to identify long-term, sustainable solutions for talent development.

Radu PREDA
Manager of Partnerships under Subsidy Projects
NXP Semiconductors Romania
TIE Steering Committee Member

TIE_{TPLUS} Contest: Academic Growth and Real-World Skills in Thermodynamic Simulation

The TIE_{TPLUS} contest is a unique opportunity for students passionate about electronic engineering and thermal simulation of electronic equipment. It focuses on using computer-aided thermodynamic simulations (CAE) to analyze and improve the thermal performance of electronic systems. By applying advanced numerical methods, participants not only sharpen essential technical skills but also prepare themselves for the challenges of today's technology-driven industries.

Why Thermodynamic CAE Simulations Matter

In modern engineering, thermodynamic Computer-Aided Engineering (CAE) simulations are a key tool for designing and optimizing technical components. They allow engineers to examine temperature distribution and heat flow in detail, helping to predict how heat will affect the performance and reliability of electronic equipment. Using methods such as Finite Element Analysis (FEA) and the Finite Volume Method (FVM), engineers can tackle real-world challenges in industries like electronics, automotive, aerospace and energy, where effective thermal management is critical.

As part of the TIE_{TPLUS} contest, students are tasked with running an advanced thermodynamic CAE simulation of an electronic product. They explore both natural convection and forced conduction scenarios, giving them hands-on experience with fundamental thermal management principles. This directly helps prevent overheating and improves the efficiency and reliability of electronic systems.

Real Benefits for Students and Future Career

TIE_{TPLUS} is more than just a competition — it's a platform for personal and professional growth. Students put their theoretical knowledge to the test while gaining valuable practical experience with modern CAE software widely used in industry. Beyond technical skills, the contest strengthens problem-solving abilities, critical thinking, and analytical reasoning — qualities highly sought after by employers.

One of the key components of the contest is writing a detailed technical report based on the simulations. This not only deepens your understanding of thermodynamic phenomena but also improves the ability to communicate technical findings clearly and effectively — a crucial skill for any engineering career.

Bridging Academia and Industry

What makes TIE_{TPLUS} stand out is its strong connection to the professional world, especially through its collaboration with Continental, a leading global company. This partnership helps bridge the gap between university and industry. Students gain insight into real industrial challenges, while companies benefit from fresh perspectives and well-prepared future engineers.

TIE_{TPLUS} is an excellent opportunity to combine academic knowledge with real-world applications, opening doors to successful careers in electronic engineering and beyond. Whether students aim for a career in R&D, design, or system optimization, this contest helps them to stand out.

Asoc. Prof. Cristian-Marcel FĂRCAŞ, Ph.D.
Technical University of Cluj-Napoca
TIE_{TPLUS} Technical Committee – Academic Trainers Chair

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Florentina STĂLINESCU, POLITEHNICA of Bucharest, Association for Promoting Electronics Technology

Wednesday, April 22

The participants are encouraged to attend any activity in any TRACK that would interest them

(except the ones marked as restricted)

Time frame	TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS – IPCEI Workshops and Trainings Events the 35th edition Industry-Wide Student Challenges	
09:00 – 14:30	***Registration (Ground floor hall)*** ***Exhibition opening & Welcome coffee*** ***(1st floor hall)***	
09:00 – 11:10	**Workshop IPCEI 1st Edition (Sustainable development of working forces for microelectronics in Romania)** ***(3rd floor, room BRD 3.08)*** ***Building Sustainable Microelectronics Packaging Talent Pipeline in Romania***	
11:10 – 11:30	***Coffee Break (1st floor hall)***	
11:30 – 13:00	**Workshop IPCEI 1st Edition (Sustainable development of working forces for microelectronics in Romania)** ***(3rd floor, room BRD 3.08)*** ***Building Sustainable Microelectronics Packaging Talent Pipeline in Romania***	
13:00 – 14:00	***Light Lunch (1st floor, Cafeteria)***	
14:00 – 18:00	**TIE$_{EPLUS}$ Final Stage (public event)** ***(Amphitheater)***	
14:00 – 18:00	**Workshop IPCEI "Microelectronics Packaging Talent and Skills for Romania: Technical meetings TIEμ, TIE$_{M\ PLUS}$ and TIE$_{T\ PLUS}$"** ***(3rd floor, room 2)***	
18:00 – 18:30	***Coffee Break (1st floor hall)***	**Steering Committee Meeting (RESTRICTED to Committee members)** ***(3rd floor, room 1)***
18:30 – 19:15	**Training IPCEI "TIE$_{EPLUS}$ SI and PI challenges in microelectronics packaging"** ***(Amphitheater)***	
19:15	***Welcome cocktail and expo networking (1st floor hall)***	

TIE 2026 Event Agenda

Thursday, April 23

The participants are encouraged to attend any activity in any TRACK that would interest them

(except the ones marked as restricted)

Time frame	TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS the 35th edition Industry-Wide Student Challenges		
08:00 – 14:00	Registration *(Ground floor hall)* Welcome coffee *(1st floor hall)*		
08:30 – *10:15*	TIE_{MPLUS} Final Stage (public event) *(1st floor, Cafeteria)*	TIE_{TPLUS} Final Stage (public event) *(3rd floor, Room 2)*	
10:15 – 10:30	*Coffee Break (1st floor hall)*		
10:30 – 12:15	TIE_{MPLUS} Final Stage (public event) *(1st floor, Cafeteria)*	TIE_{TPLUS} Final Stage (public event) *(3rd floor, Room 2)*	
12:15 – 13:15	*Lunch (Ground floor hall)*		
13:15 – 15:00	IPCEI Hands-on presentation: TIEμ Final Stage (public event) *(3rd floor, room 1)*		
15:00 – 15:15	*Coffee Break (1st floor hall)*		
15:15 – 16:00	IPCEI Hands-on presentation: TIEμ Final Stage (public event) *(3rd floor, room 1)*		
15:15 – 17:00	Committee Assessment meetings (RESTRICTED to Committee members) *(ETTI Faculty Rooms)*		
	TIE_{MPLUS}	TIE_{TPLUS}	TIEμ
15:15 – 17:00	IPCEI Hands-on and Workshop Technical Meetings		
	TIE_E *(3rd floor, room 1+2)*	TIE_M *(1st floor, room 101)*	TIEn *(1st floor, room 101BT)*
17:15 – 18:45	IPCEI Hands-on and Workshop Common Session: TIEμ, $TIE_{M\ PLUS}$ si $TIE_{T\ PLUS}$ Demystifying the resolution of the proposed topics *(Amphitheater)*		
18:45 – 20:30	Award Ceremony *(Amphitheater)*		
20:30	*Gala dinner* *(Ground floor hall)*		

Friday, April 24

The participants are encouraged to attend any activity in any TRACK that would interest them

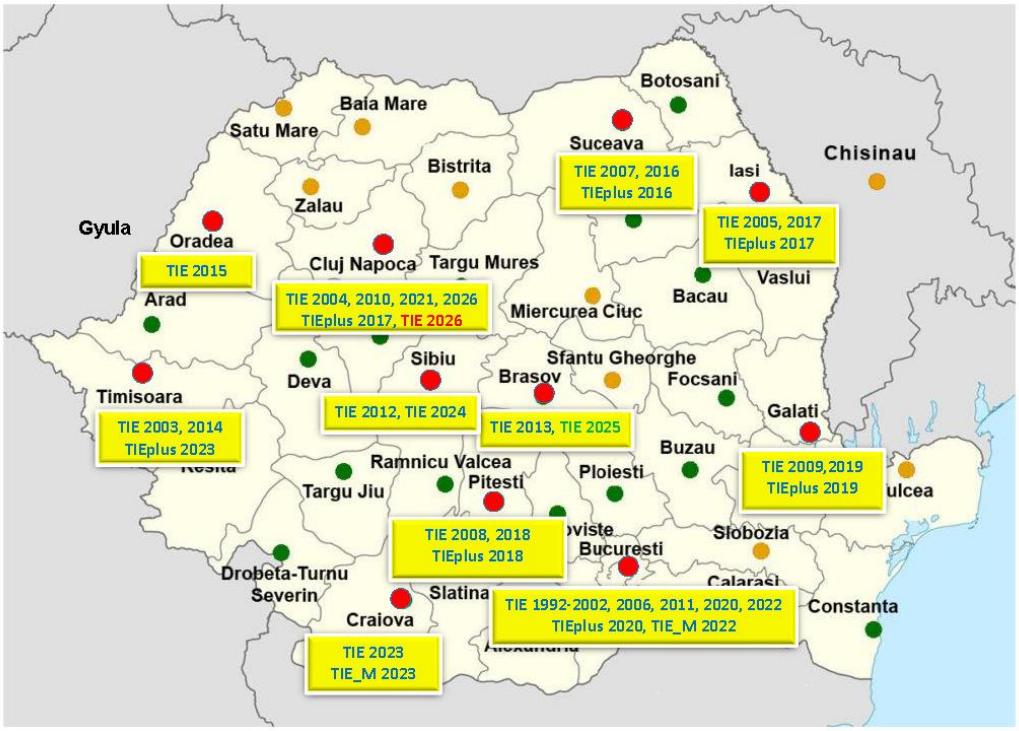
(except the ones marked as restricted)

Time frame	**TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS the 35th edition** **IPCEI Hands-on and training: Industry-Wide Student Challenges on Microelectronics Packaging**		
08:00 – 08:30	**Preliminary activities**		
	TIE_E ***(3rd floor, room 1+2)***	**TIE_M** ***(1st floor, room 101)***	**TIE_n** ***(room E04, UTCN Building)***
08:30 – 12:30	**TIE_E Hackathon** ***(3rd floor, room 1+2)***	**TIE_M Hackathon** ***(1st floor, room 101)***	**TIE_n Hackathon** ***(room E04, UTCN Building)***
12:30 – 13:30	***Lunch*** ***(Ground floor hall)***		
13:30 – 16:30	**TIE_E Assessments (public events)** ***(3rd floor, room 1+2)***	**TIE_M Assessments (public events)** ***(1st floor, room 101)***	**TIE_n Assessments (public events)** ***(room E04, UTCN Building)***
18:30 – 19:00	**TIE Steering Committee Meeting (RESTRICTED to Committee members)** ***(Amphitheater Small Room)***		
19:00	***Awarding TIE_E, TIE_M, TIE_n & Conclusion speeches*** ***(Amphitheater)*** ***Closing Ceremony & Banquet*** ***(Ground floor hall)***		

Saturday, April 25

09:30 – 10:30	**Looking Forward.** **Farwell discussion for the next TIE Industry-wide student challenge, TIE 2027** ***(1st floor hall)***

TIE past present and future editions



Year	University	Event
1992-2002	University Politehnica of Bucharest	TIE
2003	Politehnica University of Timişoara	TIE
2004	Technical University of Cluj-Napoca	TIE
2005	Gh. Asachi Technical University of Iaşi	TIE
2006	University Politehnica of Bucharest	TIE
2007	Ştefan cel Mare University of Suceava	TIE
2008	University of Piteşti	TIE
2009	Dunărea de Jos University of Galaţi	TIE
2010	Technical University of Cluj-Napoca	TIE

2011	University Politehnica of Bucharest	TIE
2012	Lucian Blaga University of Sibiu	TIE
2013	Transilvania University of Braşov	TIE
2014	Politehnica University of Timişoara	TIE
2015	University of Oradea	TIE, TIE$_{Plus}$ Kick-off
2016	Ştefan cel Mare University of Suceava	TIE, TIE$_{Plus}$
2017	Gh. Asachi Technical University of Iaşi	TIE, TIE$_{Plus}$
2018	University of Piteşti	TIE, TIE$_{Plus}$ 1st TIE bootcamp
2019	Dunărea de Jos University of Galaţi	TIE, TIE$_{Plus}$
2020	University Politehnica of Bucharest - Virtual Event	TIE, TIE$_{Plus}$
2021	Technical University of Cluj-Napoca - Virtual Event	TIE, TIE$_{Plus}$
2022	University Politehnica of Bucharest	TIE, TIE$_M$ Kick-off
2023	University of Craiova	TIE, TIE$_M$
	Politehnica University of Timişoara	TIE$_{Plus}$, TIE$_M$ $_{Plus}$
2024	Lucian Blaga University of Sibiu Aumovio Automotive Sibiu	TIE$_E$, TIE$_{Plus}$, TIE$_M$, TIE$_M$ $_{Plus}$, TIE$_T$, TIE$_\mu$
2025	Transilvania University of Braşov	TIE$_E$, TIE$_{Plus}$, TIE$_M$, TIE$_M$ $_{Plus}$, TIE$_T$, TIE$_\mu$
2026	Technical University of Cluj-Napoca	TIE$_E$, TIE$_{Plus}$, TIE$_M$, TIE$_M$ $_{Plus}$, TIE$_{TPLUS}$, TIE$_{\mu,}$ TIE$_{nano}$

Wednesday, April 22

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18:00 – 18:30	*Coffee Break (1st floor hall)*	Steering Committee Meeting (RESTRICTED to Committee members) *(3rd floor, room 1)*
18:30 – 19:15	Training IPCEI "TIE$_{EPLUS}$ SI and PI challenges in microelectronics packaging" *(Amphitheater)*	
19:15	*Welcome cocktail and expo networking (1st floor hall)*	

APTE iMAPS ROMANIA

UPSEE UP-SKILL ENGINEERING EDUCATION

UNIVERSITATEA TEHNICĂ DIN CLUJ-NAPOCA

TIE E+

10th edition

22nd of April 2026

Cluj-Napoca, Romania

TIE TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS Industry-wide Student Challenges

A WAY to turn your HOBBY into PROFESSION

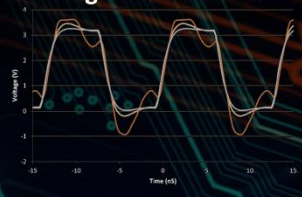
Subject and Registration!

eeCamp electrical engineering

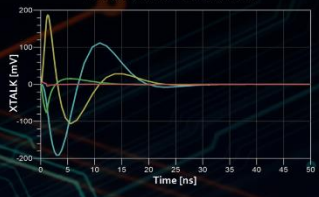
Signal & Power Integrity

Professional Student Contest

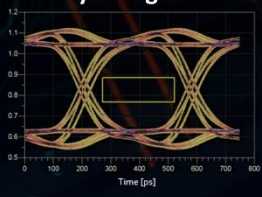
Signal Reflections



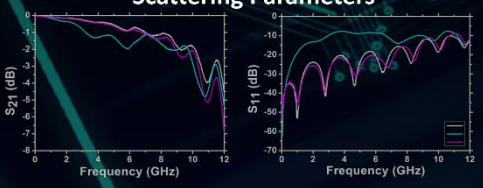
Crosstalk Noise



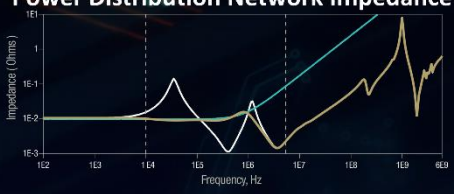
Eye Diagram



Scattering Parameters



Power Distribution Network Impedance



AUMOVIO

TIE $_{EPLUS}$ – Signal and Power Integrity challenges since 2015

Launched in 2015, TIE$_{EPLUS}$ represents an evolutionary extension of the TIE brand, focusing on virtual prototyping disciplines essential for managing the complexities of high-end PCB designs. This initiative is a strategic progression aimed at fostering PCB design expertise within the Romanian electronics community. Building on the foundational knowledge acquired in the TIE$_{E}$ contest, which covers the intricacies of PCB layout interconnect design, TIE$_{EPLUS}$ shifts the spotlight to the critical analysis of signal and power integrity across these interconnects. Contestants are tasked with generating both pre-layout recommendations and post-layout evaluations of a given electronic module, thus demonstrating a deeper engagement with the engineering design process.

More than a competition, TIE$_{EPLUS}$ is a comprehensive educational platform that encourages students to not only assimilate new knowledge but polish highly sought-after skills. Defending their design solutions before the TIE$_{EPLUS}$ committee offers a unique opportunity for participants to enhance their analytical abilities and refine their presentation and discussion skills. This interaction underlines the multifaceted nature of PCB design, requiring a balance between performance, design constraints, and cost considerations – factoring in the technology employed in PCB fabrication and the design resources at hand.

Participating in and training for TIE$_{EPLUS}$ challenge, students are learning and developing skills needed in the industry such as:

- using and generating scattering parameters (s-parameters),
- understanding a digital interface signal timing
- properly configuring an IBIS driver and receiver to characterize or analyze a transmission channel
- defining eye-diagram and s-parameters masks
- designing PCB stack-up for high-speed signals and power-integrity
- providing pre-layout guidance for high-speed trace routing (e.g., trace dimensions, length matching strategies, via design, crosstalk analysis) and power delivery network (PDN) (e.g., DC voltage drop, AC budget analysis, decoupling capacitor strategy)
- post-layout analysis for identifying and proposing solutions to possible signal or power delivery issues in a digital interface final design

- understanding physical parameters effect over electromagnetic wave propagation
- understanding simulation parameters influence over obtained results

The TIE$_{EPLUS}$ challenge unfolds through a structured sequence of steps, designed to facilitate an engaging and educative experience for the students, while trying to emulate the typical engineering design process prevalent in the electronics industry:

- Subject Announcement – An overview of the TIE$_{EPLUS}$ theme and main topics of the subject are made available online. This gives students ample opportunity to deepen their understanding of specific digital interfaces or technologies.

- Student Enrollment – The committee conducts a thorough review of all registration submissions to ensure a level playing field. Candidates with extensive experience in SI/PI are carefully screened to maintain the competition's focus on developing talent.

- Challenge Resolution – Participants are granted a two-week period to solve the given challenge and craft their technical solutions, submitted in the form of an R&D report.

- Solution Evaluation – Following submission, contestants are expected to prepare and deliver a concise presentation (lasting 15-20 minutes) to the technical committee.

This approach not only prepares participants for the rigorous demands of the electronics design industry but also ensures that each phase of the challenge is an opportunity for learning, skill enhancement, and meaningful feedback, underscoring the competition's role as a bridge between academic learning and professional application.
The core challenge lies in effectively integrating signal integrity (SI) analysis with power distribution network (PDN) considerations. This involves ensuring that signals are transmitted with minimal distortion and interference, while also managing the power delivery to all the components in the system, to guarantee stable and reliable operation.

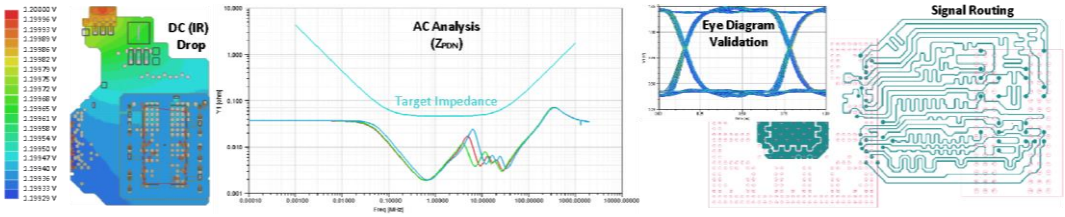


Figure 1 Subject highlights

In the evaluation phase of the contest, a panel comprised of experts from both the industrial sector and academic institutions comes together to meticulously review the R&D reports submitted by contestants. Prior to the oral presentations, each evaluator dedicates time to thoroughly examine the reports, formulating precise inquiries focused on the methodology and clarity of the results derived from the simulation processes.

The evaluation is structured around three core competencies:

- Software Proficiency – Examining the participant's ability to effectively employ the available simulation tools and configure the appropriate settings for accurate results.
- Theoretical Insight – Assessing the contestant's understanding of the physical principles and phenomena that are fundamental to the topics being investigated.
- Solution Excellence – Evaluating the originality, practicality, and technical soundness of the proposed solution, including how well it addresses the challenge presented.

To be recognized by the TIE$_{EPLUS}$ committee as proficient in the SI/PI domain and to be awarded a diploma, participants must demonstrate broad understanding across a wide array of topics and successfully address more than half of the subject requirements. This process ensures a rigorous standard of competence and also mirrors the professional evaluation methodologies used in industry and academia, fostering a realistic and constructive environment for learning and recognition.

Marcel MANOFU,
AUMOVIO Technologies Romania,
Timișoara
TIE$_{EPLUS}$ Committee Chair

Mihai DĂRĂBAN,
Technical University
of Cluj-Napoca
TIE$_{EPLUS}$ Committee Co-Chair

TIE$_{EPLUS}$ Committee

Chair:
Marcel MANOFU, AUMOVIO Technologies Romania, Timişoara
Co-Chair:
Mihai DĂRĂBAN, Technical University of Cluj-Napoca

Technical Committee – Academic Trainers
Chair:
Mihai DĂRĂBAN, Technical University of Cluj-Napoca

Members:
Arcadie CRACAN, Gh. Asachi Technical University of Iaşi
Mădălin MOISE, POLITEHNICA of Bucharest
Gheorghe PANĂ, Transilvania University of Braşov

Industrial Committee
Chair:
Marcel MANOFU, AUMOVIO Technologies Romania, Timişoara
Co-Chair:
Radu VOINA, KEYTEK Innovation, Alba Iulia

Members:
Cosmin MOISĂ, AUMOVIO Technologies Romania, Timişoara
Cătălin NEGREA, Darknote Engineering
Mihai RUS, Aumovio Engineering Services
Roxana VLĂDUȚĂ, Marvell Technology

Final Stage participants:

Mihai-Constantin COITA	Politehnica University of Timisoara
Mihai-Vasile POPESCU	Politehnica University of Timisoara
Vlad-Andrei CRISTESCU	Technical University of Cluj-Napoca
Aleksandar TRIFUNOVIC	University of Novi Sad
Filip LAZIC	University of Novi Sad
Andrei ACSINTE	Ștefan cel Mare University of Suceava

Thursday, April 23

The participants are encouraged to attend any activity in any TRACK that would interest them

(except the ones marked as restricted)

Time frame	**TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS the 35th edition Industry-Wide Student Challenges**		
08:00 – 14:00	**Registration** ***(Ground floor hall)*** **Welcome coffee** ***(1st floor hall)***		
08:30 – *10:15*	**TIE$_{MPLUS}$ Final Stage (public event)** ***(1st floor, Cafeteria)***	**TIE$_{TPLUS}$ Final Stage (public event)** ***(3rd floor, Room 2)***	
10:15 – 10:30	***Coffee Break*** ***(1st floor hall)***		
10:30 – 12:15	**TIE$_{MPLUS}$ Final Stage (public event)** ***(1st floor, Cafeteria)***	**TIE$_{TPLUS}$ Final Stage (public event)** ***(3rd floor, Room 2)***	
12:15 – 13:15	***Lunch*** ***(Ground floor hall)***		
13:15 – 15:00	**IPCEI Hands-on presentation: TIEμ Final Stage (public event)** ***(3rd floor, room 1)***		
15:00 – 15:15	***Coffee Break*** ***(1st floor hall)***		
15:15 – 16:00	**IPCEI Hands-on presentation: TIEμ Final Stage (public event)** ***(3rd floor, room 1)***		
15:15 – 17:00	**Committee Assessment meetings (RESTRICTED to Committee members)** ***(ETTI Faculty Rooms)***		
	TIE$_{MPLUS}$	**TIE$_{TPLUS}$**	**TIEμ**
15:15 – 17:00	**IPCEI Hands-on and Workshop Technical Meetings**		
	TIE$_{E}$ ***(3rd floor, room 1+2)***	**TIE$_{M}$** ***(1st floor, room 101)***	**TIEn** ***(1st floor, room 101BT)***
17:15 – 18:45	**IPCEI Hands-on and Workshop Common Session: TIEμ, TIE$_{M\ PLUS}$ si TIE$_{T\ PLUS}$ Demystifying the resolution of the proposed topics** ***(Amphitheater)***		
18:45 – 20:30	**Award Ceremony** ***(Amphitheater)***		
20:30	***Gala dinner*** ***(Ground floor hall)***		

APTE iMAPS ROMANIA

UPSEE UP-SKILL ENGINEERING EDUCATION

UNIVERSITATEA TEHNICĂ DIN CLUJ-NAPOCA

TIE 4th edition M+

23rd of April 2026

Cluj-Napoca, Romania

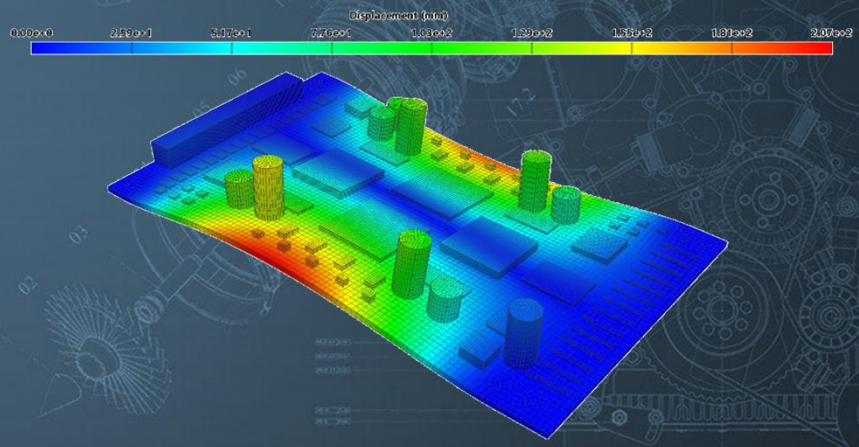
TIE TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS Industry-wide Student Challenges

A WAY to turn your HOBBY into PROFESSION

Subject and Registration!

eecamp electrical engineering

Professional Structural Analysis Contest for Students



AUMOVIO

INAS power to change

TIE-M Plus: Shape the Future of Engineering with FEA

Finite Element Analysis (FEA) is a numerical method widely employed to predict the behavior of structures and assemblies under prescribed physical conditions. It provides a systematic framework for analyzing complex physical phenomena—including solid and fluid mechanics, heat transfer, electromagnetics, and acoustics—which are typically governed by Partial Differential Equations (PDEs). The inherent complexity of these equations has led to the development of advanced numerical techniques over recent decades, among which FEA has emerged as one of the most robust and versatile approaches.

Due to its predictive accuracy and computational efficiency, FEA has become an indispensable tool across a broad range of engineering disciplines. Its advantages include enhanced insight into critical design parameters, the ability to perform virtual prototyping, a reduced reliance on experimental validation, and the facilitation of shorter and more cost-effective design cycles.

In this context, the TIE-M+ initiative, introduced in 2023, represents a dedicated effort to promote the application of structural simulation methods in the field of electronic packaging. The competition is designed to provide students with comprehensive exposure to structural integrity assessment within electronics development.

Participants are tasked with analyzing electronic modules - such as control units and sensors - derived from industrial and automotive applications. The assigned problems require the identification of structural vulnerabilities, the formulation of appropriate numerical modeling strategies, and the execution of simulations addressing phenomena such as printed circuit board (PCB) deformation, solder joint reliability, and dynamic behavior (e.g., eigenfrequency and vibration analysis). Furthermore, participants are expected to propose design optimization strategies aimed at improving overall system performance.

Fig. Example of a product proposed for the simulation contest

The primary objective of the competition is to develop fundamental competencies in numerical simulation, encompassing model preparation, boundary condition definition, result interpretation, and design optimization. Additionally, the initiative seeks to familiarize participants with state-of-the-art, multidisciplinary workflows representative of current industrial practice, thereby contributing to the professional development of future engineers in the field of electronics design and reliability.

Tamas KRAUSZ, AUMOVIO Technologies Romania, Romania
TIE$_{MPLUS}$ Committee Chair

Dragoș Apostol, Politehnica Bucharest, Romania

TIE$_{MPLUS}$ Committees

Chair:
Tamas KRAUSZ, AUMOVIO Technologies Romania
Co-Chair:
Daniel COMEAGĂ, POLITEHNICA Bucharest

Technical Committee – Academic Trainers
Chair:
Dragoș APOSTOL , National University of Science and Technology Politehnica Bucharest
Members:
Sergiu Valentin GALAȚANU, Politehnica University of Timişoara
Mircea Cristian DUDESCU, Technical University of Cluj-Napoca
Ioana Alexandra RAD, Technical University of Cluj-Napoca
Ștefan SOROHAN, National University of Science and Technology Politehnica Bucharest
Mihai COSTEA, National University of Science and Technology Politehnica Bucharest

Industrial Committee

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Ionut VERZEȘ, AUMOVIO Technologies Timișoara

Members:
Iulia ȚINCA, Infineon Technologies AG
Ionuț AILINEI, AUMOVIO Technologies Romania SRL
Răzvan STANCA, INAS SA

Final Stage participants:

Vlad NIȚOIU	National University of Science and Technology Politehnica Bucharest
David CRAIOVEANU	National University of Science and Technology Politehnica Bucharest
Alexandru TURTA-MORARIU	Politehnica University of Timişoara
Darius-Ștefan LICIU	Politehnica University of Timişoara

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UPSEE UP-SKILL ENGINEERING EDUCATION

UNIVERSITATEA TEHNICĂ DIN CLUJ-NAPOCA

TIE T+

4th edition

23rd of April 2026

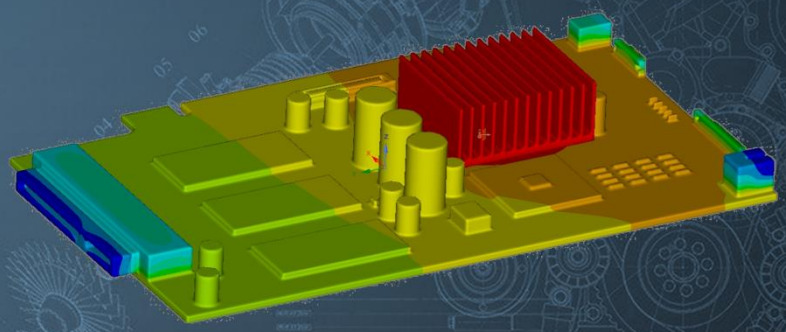
Cluj-Napoca, Romania

TIE TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry-wide Student Challenges
A WAY to turn your HOBBY into PROFESSION

Subject and Registration!

eecamp electrical engineering

Professional Thermal Management Contest for Students



AUMOVIO

INAS power to change

Thermal-Dynamic CAE Simulation: An Advanced Approach for Analyzing the Thermal Behavior of Technical Systems

Thermal-dynamic Computer-Aided Engineering (CAE) simulation is an advanced technique used to analyze the thermal behavior of technical systems and components under variable operating conditions. It combines thermal and dynamic analysis to provide a comprehensive view of how heat transfer and temperature fluctuations affect mechanical performance, operational efficiency, and long-term reliability of the system.

In modern engineering, thermal-dynamic CAE simulation plays a crucial role in evaluating and optimizing the performance of technical systems. By applying state-of-the-art numerical methods such as Finite Element Analysis (FEA) and Finite Volume Method (FVM), this technique allows for a detailed assessment of temperature distribution and thermal flows, as well as their impact on the materials and structures involved.

The use of FEA and FVM in thermal-dynamic CAE simulation enables detailed analysis of the thermal behavior of systems. These methods contribute to optimizing heat dissipation processes, preventing overheating, and ensuring safe and efficient operating conditions.

In the industrial sector, thermal-dynamic CAE simulation is essential for designing and validating thermal components used in fields such as automotive, aerospace, energy, and electronics. Temperature fluctuations can significantly impact the durability and performance of systems, and thermal-dynamic CAE simulations not only reduce costs associated with physical prototypes but also accelerate product development by quickly identifying problems and optimizing technical solutions.

Any system that generates or interacts with heat sources must efficiently manage heat removal to prevent overheating and performance losses. Thermal simulations are crucial in designing cooling solutions such as radiators, heat exchangers, and ventilation systems, contributing to their improved efficiency.

By using thermal simulations, thermal behavior issues can be identified and corrected during the design phase, thus reducing the need for physical tests and costly prototypes. This process leads to significant savings in time and financial resources, accelerating the product development cycle.

Many components and systems are designed to operate in extreme or variable temperature environments, such as those in the aerospace, space, or industrial sectors. Thermal simulations allow for the evaluation of the performance of these components

under conditions that would be difficult to replicate in physical experiments, thus ensuring their reliability in real operating conditions.

Now in its third edition, the TIE_{MPLUS} competition aims to promote the use of CAE simulations among students from various technical faculties in Romania. Through this initiative, participants can demonstrate their skills in performing complex thermodynamic simulations by applying advanced numerical analysis methods. The competition also contributes to the development of technical skills of future engineers and familiarizes them with the software tools used in the industry to optimize the thermal behavior of technical systems.

Competitors must perform a thermodynamic simulation using CAE tools, thermally evaluating a product with four electronic components in a climate chamber environment, using natural convection and forced conduction. Based on the obtained thermal simulations, they will write a detailed report. This report will serve as the basis for analyzing and evaluating the competitors, thus determining the performance and efficiency of the proposed technical solutions.

Thermal-dynamic CAE simulation is an indispensable method in modern engineering, providing a detailed and optimized evaluation of the thermal behavior of technical systems. By applying advanced numerical methods, this technique contributes to improving the performance, efficiency, and reliability of systems, reducing costs and development time. The TIE_{MPLUS} competition offers students the opportunity to directly experience these benefits, consolidating their knowledge and preparing them for future technical challenges.

Cristina Mihaela DRĂGAN,
Aumovio Autonomous Mobility Romania
TIE_{TPLUS} – Committee Chair

Cristian-Marcel FĂRCAŞ,
Technical University of Cluj-Napoca
TIE_{TPLUS} Technical Committee –
Academic Trainers Chair

TIE$_{TPLUS}$ - Committee

Chair:
Cristina-Mihaela DRĂGAN, AUMOVIO Technologies Romania SRL

Technical Committee – Academic Trainers
Chair:
Cristian FĂRCAŞ, Technical University of Cluj Napoca
Members:
Cristian FARCAŞ, Technical University of Cluj Napoca
Raul IONEL, Politehnica University Timisoara
Dorin LELEA, Politehnica University Timisoara
Ciprian IONESCU, Politehnica Bucharest, Romania

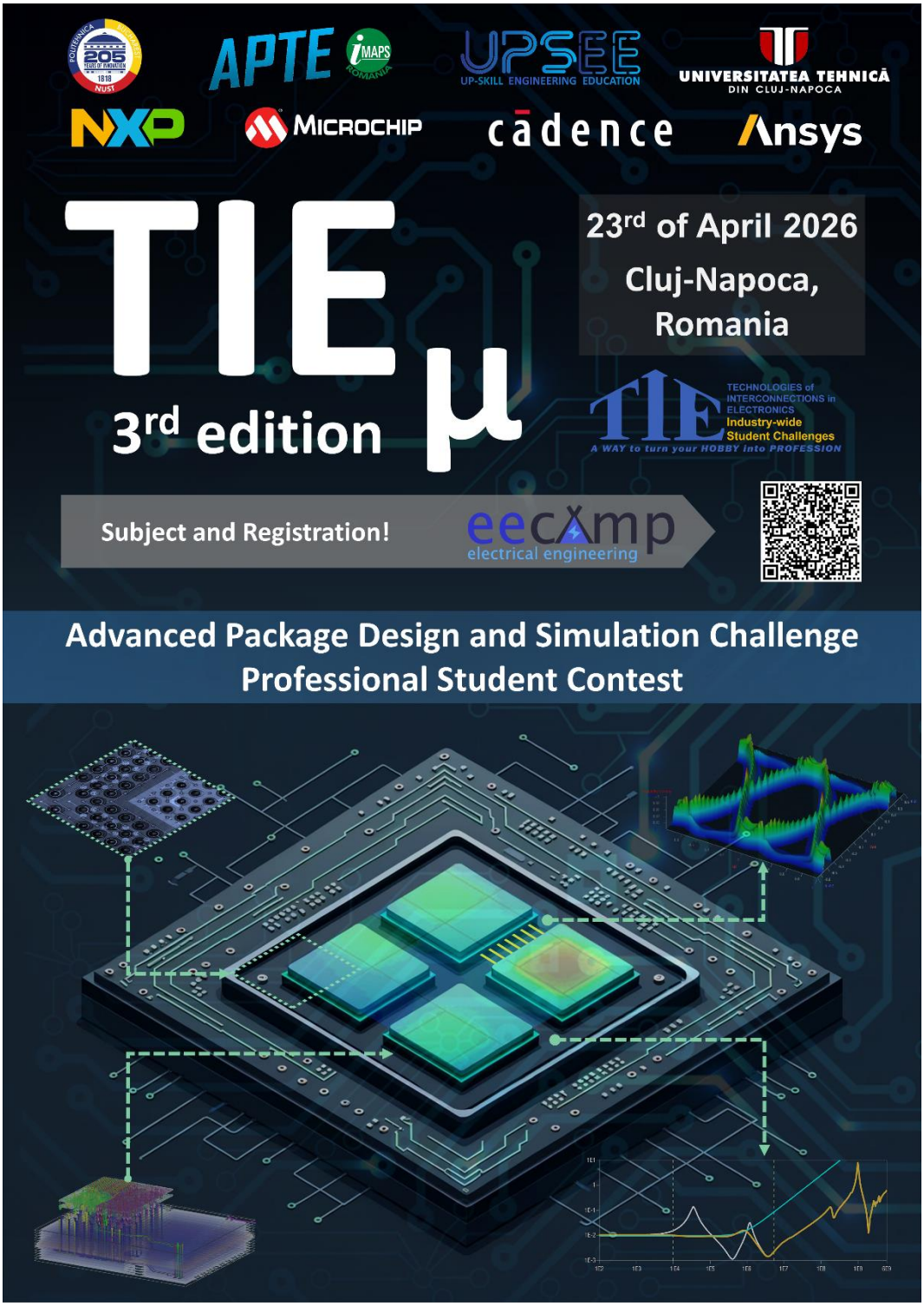
Industrial Committee
Co – Chair:
Constatin POPESCU, AUMOVIO Technologies Romania SRL
Members:
Cristina-Mihaela DRĂGAN, AUMOVIO Technologies Romania SRL
Constatin POPESCU, AUMOVIO Autonomous Mobility Romania SRL
Lucian BODIN, AUMOVIO Autonomous Mobility Romania SRL
Razvan STANCA, INAS SA Craiova

TIE$_{Tplus}$ Winners

Year	Name	University
2025	Daniel Andrei BULUGHEANĂ	Technical University of Cluj Napoca
2024	Alexandru-Gabriel MIHAL	Politehnica University of Timişoara
2023		

Final Stage participants:

Alexandru Andrei Popovici	Technical University of Cluj Napoca
Alin Tantau	Technical University of Cluj Napoca
Andreea Georgiana Nastuta	Technical University of Cluj Napoca
Emanuel Handra	Politehnica University of Timişoara
George Danile Ghita	POLITEHNICA Bucharest
Mihai Florin Bizdadea	POLITEHNICA Bucharest


APTE
iMAPS ROMANIA
UPSEE
UP-SKILL ENGINEERING EDUCATION
UNIVERSITATEA TEHNICĂ
DIN CLUJ-NAPOCA
NXP
MICROCHIP
cadence
Ansys
TIE μ
3rd edition
23rd of April 2026
Cluj-Napoca,
Romania
TIE
TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry-wide Student Challenges
A WAY to turn your HOBBY into PROFESSION
Subject and Registration!
eeCamp
electrical engineering
Advanced Package Design and Simulation Challenge
Professional Student Contest

TIEμ 2026 - third edition of industry-wide student challenge
Shaping the next generation of professional SiP designers

Gordon Moore famously predicted in his" Moore's Law" paper that it might become more cost-effective to construct extensive systems using smaller, individually packaged functions interconnected together. More than half a century later, the structure of the System-on-a-Chip (SoC) changes significantly with the partitioning of a monolithic die into smaller chiplets: packaging becomes one of the main focuses when designing a chip and the way the initial functionality is partitioned between multiple chiplets and how these are interconnected means we must shift our perspective to Systems in Package (SiP) (source: A. Jâjâie, A. Puşcaşu, I. Ailenei, C. B. Ciobanu and P. Svasta, "Chiplets and Next-gen Packaging Technologies in University Education," 2023 IEEE 29th International Symposium for Design and Technology in Electronic Packaging (SIITME), Craiova, Romania, 2023, pp. 207-214, https://doi.org/10.1109/SIITME59799.2023.10431355)

As the industry shifts towards heterogeneous integrations, systems in package and chiplets it becomes of paramount importance to train future engineers in these state-of-the-art techniques, including employing interposers, 2.5D, and 3D integration.

Starting in 2024, TIE introduced a new topic – TIEμ (C. Ciobanu, D. Manolescu, R. Vlăduţă, L. Chiţu, C. Moisă, M. Manofu and P. Svasta, "TIE Micro – Chiplets and Next-gen Packaging," 2024 IEEE 30th International Symposium for Design and Technology in Electronic Packaging (SIITME), Sibiu, Romania, 2024, pp. 504-511,

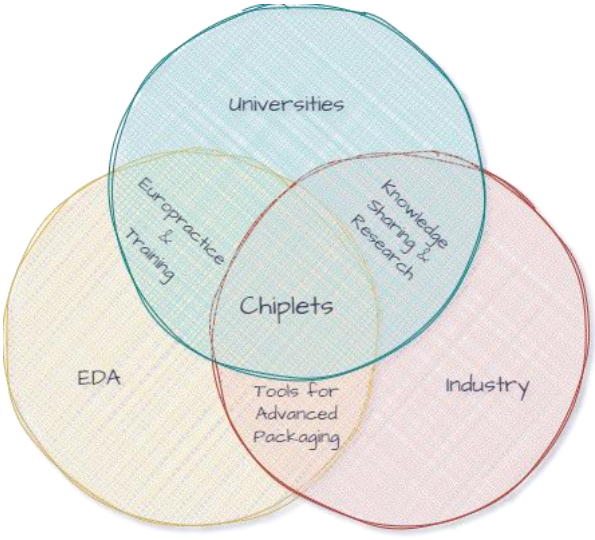


Figure 1 *Interaction between Industry, Universities and Chiplets*

https://doi.org/10.1109/SIITME63973.2024.10814902), which is addressing important subjects such as advanced packaging, 2.5D/3D integration and chiplets. In this regard, TIE is a unique approach and to our knowledge the only one of this type in Europe which bridges the gap between Universities, Industry and advanced topics such as Chiplets as shown in Figure 1. The contest brings all stakeholders to the table, ensuring industry relevant data sets are proposed as topics using state of the art EDA tools in an academic environment, in order to introduce future engineers to an upcoming future career path in advanced packaging, chiplet integration and heterogenous design.

As illustrated in Figure 2 (source: https://www.nature.com/articles/s41928-024-01126-y), the modern approach for heterogenous integration requires high speed interfaces such as Universal chiplet interconnect express (UCIe) and advanced packaging. TIEµ focuses on the new interconnection challenges for high-speed interfaces, interposers and other techniques the students need to prepare for when transitioning from SoC to SiPs. SiPs make use of specialized chiplets with customer IP and memory on the same package.

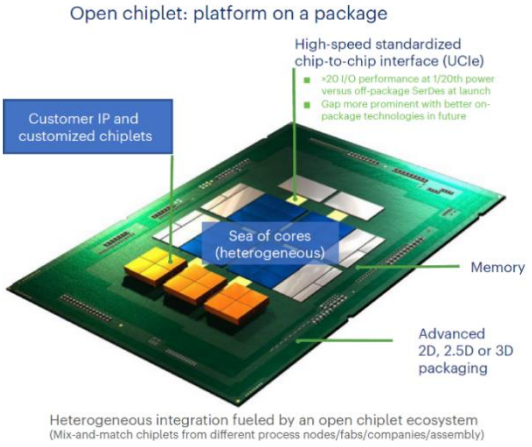
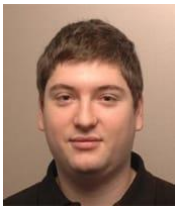


Figure 2 Heterogeneous open chiplet on-package

The main topics necessary for designing advanced packaging and interconnects include insight in layout design (package or PCB), signal and power integrity, system in package (*SiP)* fundamentals, timing and high frequency analysis.

Dan MANOLESCU, 2D Photonics

TIEµ - Committee Chair



Cătălin CIOBANU, Transilvania University of Brașov,
National Institute for Research and Development in Microtechnologies - IMT Bucharest
TIEµ - Committee Co-Chair

TIE$_{\mu}$ - Committee

Chair:
Dan MANOLESCU, 2D Photonics
Co-Chair:
Cătălin CIOBANU, Transilvania University of Braşov

International Modelling & Simulation Environment Coordinator
Raul FIZEȘAN, Technical University of Cluj-Napoca

Technical support IT Department from Technical University of Cluj-Napoca
Chair:
Claudiu IAKKEL, Comunication Center PUSZTAI KALMAN

Members:
Cristinel Mihai MOCAN, Comunication Center PUSZTAI KALMAN
Andraş NYAKAS, Comunication Center PUSZTAI KALMAN

Technical Committee – Academic Trainers
Chair:
Cătălin CIOBANU, Transilvania University of Braşov
Co-Chair:
Raul FIZEȘAN, Technical University of Cluj-Napoca

Members:
Diana BRÎNARU, POLITEHNICA of Bucharest
Arcadie CRACAN, Gh. Asachi Technical University of Iaşi
Aurel GONTEAN, Politehnica University of Timişoara
Csaba Zoltán KERTÉSZ, Transilvania University of Braşov
Mihaela PANTAZICĂ, POLITEHNICA of Bucharest

Industrial Committee
Chair:
Dan MANOLESCU, 2D Photonics
Co-Chair:
Iosif ANTOCHI, NXP Romania

Members:
Ciprian ABRAMOV, Brainiac Engineering, Bucharest
Dorin ANTONOVICI, IFM Sibiu
Marcel MANOFU, AUMOVIO Technologies Romania,, Timișoara
Vladimir PAPIC, Cadence Design Systems
Mihai SAIN, Microchip Technology București
Ciprian VASILE, Association for Promoting Electronics Technology
Roxana VLADUTA, Marvell Technology

TIE$_{\mu}$ Winners

2025	Alexandru-Andrei ALEXA	POLITEHNICA of Bucharest
2024	Adelina CÎRLAN	POLITEHNICA of Bucharest

Final Stage participants:

Alexandru Cimpean	Technical University of Cluj Napoca
Andrei Pătrașcu	POLITEHNICA Bucharest
Călin Ciorici	Gh Asachi Technical University of Iași
George Cristian Rotaru	POLITEHNICA Bucharest
Octavian-Constantin Axinte	Technical University of Cluj Napoca
Soos Gyorffy Bence	Technical University of Cluj Napoca

Friday, April 24

The participants are encouraged to attend any activity in any TRACK that would interest them

(except the ones marked as restricted)

Time frame	**TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS the 35th edition** **IPCEI Hands-on and training: Industry-Wide Student Challenges on Microelectronics Packaging**		
08:00 – 08:30	**Preliminary activities**		
	TIE$_E$ *(3rd floor, room 1+2)*	**TIE$_M$** *(1st floor, room 101)*	**TIE$_n$** *(room E04, UTCN Building)*
08:30 – 12:30	**TIE$_E$ Hackathon** *(3rd floor, room 1+2)*	**TIE$_M$ Hackathon** *(1st floor, room 101)*	**TIE$_n$ Hackathon** *(room E04, UTCN Building)*
12:30 – 13:30	***Lunch*** *(Ground floor hall)*		
13:30 – 16:30	**TIE$_E$ Assessments (public events)** *(3rd floor, room 1+2)*	**TIE$_M$ Assessments (public events)** *(1st floor, room 101)*	**TIE$_n$ Assessments (public events)** *(room E04, UTCN Building)*
18:30 – 19:00	**TIE Steering Committee Meeting (RESTRICTED to Committee members)** *(Amphitheater Small Room)*		
19:00	***Awarding TIE$_E$, TIE$_M$, TIE$_n$ & Conclusion speeches*** *(Amphitheater)* ***Closing Ceremony & Banquet*** *(Ground floor hall)*		


TIE
TIE E
35th Edition
University Professional
Electronics Packaging
CAD Contest for Students
April 24, 2026
Cluj Napoca, Romania
POLITEHNICA BUCUREȘTI
1818
APTE
TECHNICAL
UNIVERSITY
OF CLUJ-NAPOCA
ROMANIA
A WAY to turn your HOBBY into a PROFESSION

TIE$_E$, migration in to Industry-Wide student challanges

In the Romanian electronics field, one of the main results of the partnership between academia and industry is the TIE$_E$ Professional Student Contest. This partnership result aims to challenge the students, year after year, to develop their abilities in CAD techniques for development of printed circuits (PCB) and electronic modules. The entire process, from designing a component with symbol and footprint, to an entire PCB with a lot of constraints and design rules, followed by the necessary fabrication files, is emphasized with this contest. Best 30…40 students from Romanian universities, and not only, are welcomed every year to solve the difficult tasks developed by industry and academia. The contest's subjects are annually updated to reflect the latest technological advancements in the industry.

Distinguished experts in electronics packaging from various companies, who form the Industrial Advisor Committee – IAC [1], work closely with academia . Together, they have significantly contributed to essential components of the competition: the subject and the evaluation scale. By doing so, the engineers involved in organizing the contest voluntarily aim to provide today's students with the kind of support and opportunities they received during their university years.
One of the TIE$_E$ main objectives is to grow a robust community dedicated to providing young and enthusiastic students with a platform to showcase the skills they have gained through their coursework, internships, and personal interests.
The main theoretical and engineering aspects that need to be assumed by participating students, include:

- designing symbols and footprints as well as the link between them;
- understanding datasheets and extracting the necessary information;
- PCB stack-up, electrical/non-electrical layers definition;
- mechanical constrains;
- thermal considerations;
- basic signal and power integrity concepts;
- placement strategies;
- routing strategies and styles;
- fabrication files creation (Gerber, N. C. Drill, BOM, assembly drawings) and their meaning.

An increasing number of students are participating in the TIE event, likely due to the numerous benefits it offers. Taking part in TIE allows students to showcase their projects to industry experts and potential employers, significantly enhancing their career prospects through increased visibility and valuable networking opportunities. Additionally, the top-performing students receive valuable certifications that confirm their proficiency in PCB design, a crucial skill in hardware engineering [1]. These

certificates, recognized by leading tech companies, serve as a passport to excellent career opportunities.

All students participating in TIE$_E$ professional contest are selected, by their academic trainers, from local contest phases. Before the contest, students might get some work packages from the organizers, to prepare for the contest, like symbols and footprints to be able to reach PCB layout phase much faster. The subject is composed from a schematic diagram which must be completed with CAD SW with 100% fidelity and a list of requirements, split into 3 parts, related to:

- library definition and schematic design;
- PCB technology, rule definition and placement and routing requirements, layout design;
- thermal management and manufacturing documentation.

Every year, the industrial committee aims to introduce new elements in the competition subject, in line with the latest trends from the today's industry:

- professional project library handling;
- antenna routing;
- flex-rigid stack-up;
- edge connectors;
- new requirements for SI/PI and SIP BGA fanout;
- specific design for manufacturing (DFM) requirements.

Each contestant is evaluated by a combined team formed by 2 or 3 members from the industry and academia, based on an evaluation scale, which is developed by the Technical Committee [TC] in collaboration with academic trainers, ensuring at the same time a clear, impartial and transparent ranking. TIE$_E$ and, finally, the whole TIE event and environment, is the proof of the voluntary joint efforts of academia and industry. This collaboration offers well prepared future engineers for the current industry challenges and the next generation of academic staff.
During the evaluation, the focus is on the comprehensive assessment of a PCB design's quality and accuracy. The evaluation process hinges on several critical factors, starting with the precise identification of components, pads, pins, footprints, and nets. Every element must align with contest-specific regulations, which may include requirements for differential pair configurations, PCB stack-up arrangements, and strict clearance and width specifications. In addition, the accurate placement of key components, such as decoupling capacitors, is essential for maintaining electrical performance. Proper routing of interconnections must respect Design for Manufacturability (DFM) and Signal Integrity (SI) principles, ensuring optimal functionality and efficiency. Thermal management is also crucial, requiring thorough calculations to prevent overheating for components or traces. Finally, the generation of complete and detailed fabrication files plays a pivotal role in transitioning the design from concept to production. This step aims to provide a

structured framework for evaluating each of these critical aspects, ensuring that the design adheres to industry standards and project requirements.

All these engineering efforts evaluated by TC & IAC [1], are ranked in an order dictated by the accumulated points by each participant. According to these points, IAC establishes certifications in accordance with the scores achieved after the evaluation of participants. There are 2 types of certifications, awarded by the chairman of TIE$_E$: Schematic designer & PCB designer

The dedication of academic institutions in developing an environment for students to explore and innovate, coupled with the constant support from industry experts who provided practical insights and cutting-edge technologies has elevated the TIE$_E$ competition to a Industry-Wide student challenge. This partnership between academia and industry has created an exceptional growth opportunity, where theoretical knowledge is seamlessly integrated with real-world applications, preparing the next generation of engineers for the challenges of the future. The commitment to excellence and mentorship has not only shaped the future careers of participants, but also advanced the field, setting a new standard for future collaborations.

[1] Mihai Cenușă; Liviu Viman et all, "Advanced Collaboration in the Romanian Electronics Field based on the TIE Professional Student Contest," 2024 IEEE 30th International Symposium for Design and Technology in Electronic Packaging (SIITME), Sibiu, Romania, 2024, pp. 487-493, doi: 10.1109/SIITME63973.2024.10814785.

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Recognition by the industry of student competences in PCB design

TIE 2026 Certificate of Competence

The „PCB Designer" certificate is awarded, after evaluation, by the TIE IC (Industrial Committee) to selected contestants, as recognition of their high level of knowledge in the field of EDA and CAD for development of electronic modules/assemblies. The evaluation is based on the worldwide known and accepted IPC standards. The certificate is offered under the "umbrella" of the Association for Promoting Electronics Technology (APTE).

Please see more details on www.apte.org.ro.

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2020	Victor ȚURCA	Ştefan cel Mare University of Suceava
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2018	Alexandru Nicolae GOGLEA	University of Piteşti
2017	Gheorghe COJOCARIU	Ştefan cel Mare University of Suceava
2016	Radu VOINA	Technical University of Cluj Napoca
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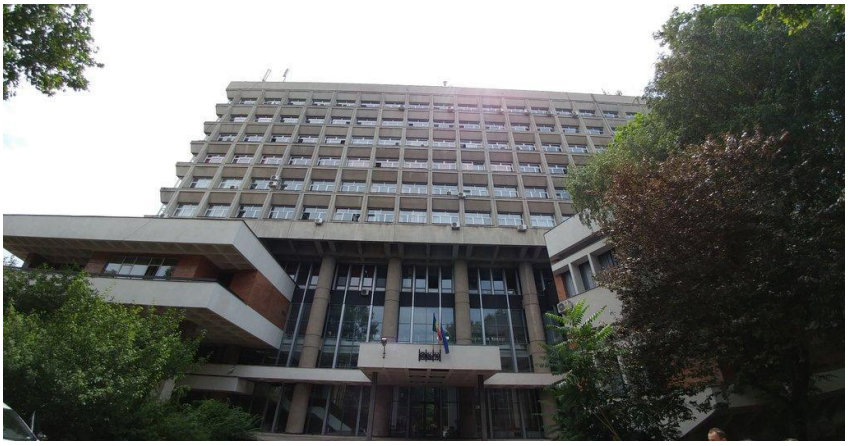

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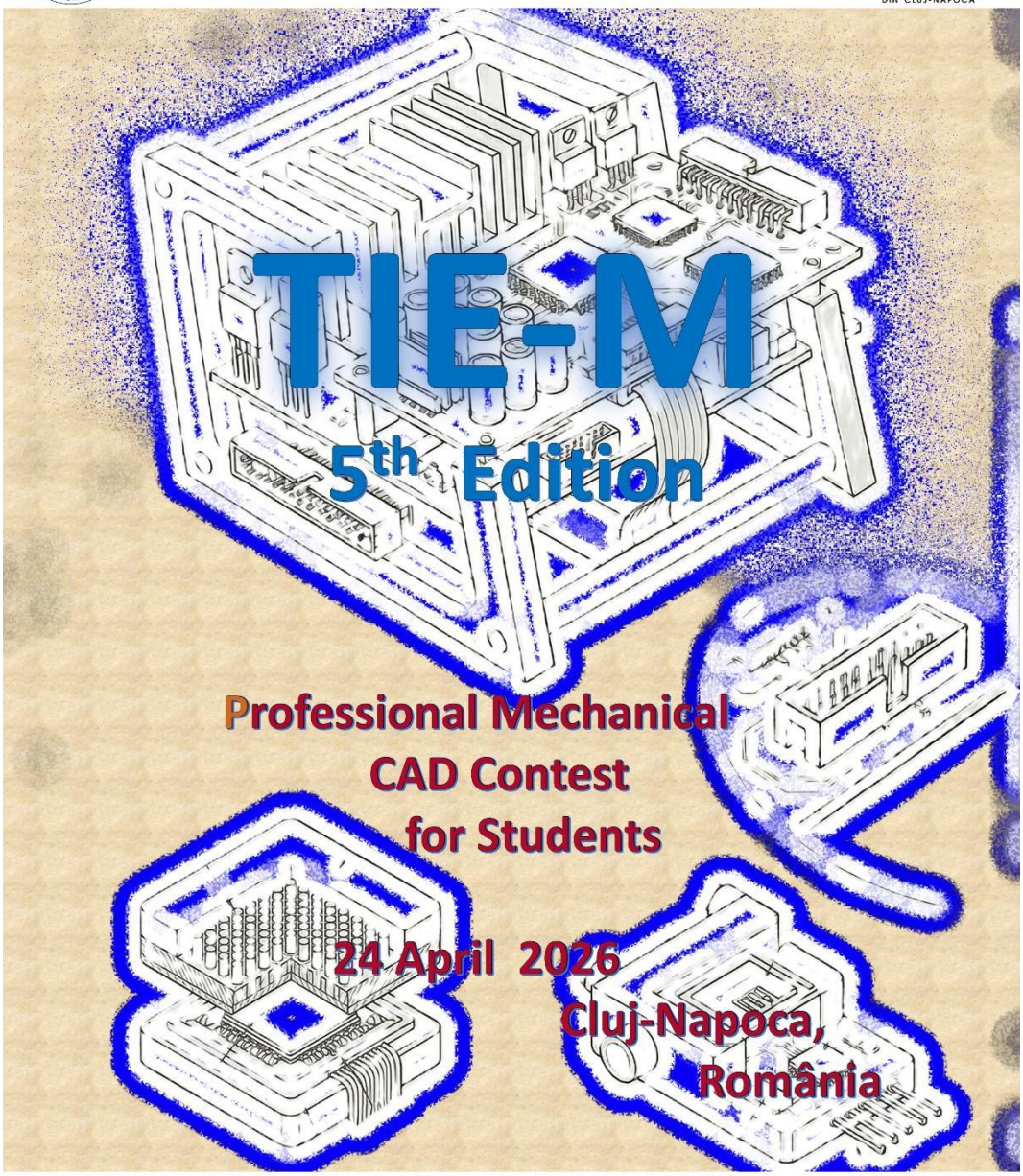

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www.tie.ro

TIE$_M$ -Mechanical

TIE$_M$ - Mechanical is a CAD Design Challenge that aims to assess students' proficiency in computer-aided design (CAD) for mechanical components, with a focus on electronic packaging and electro-mechanical assembly as shown in Figure 1. This challenge evaluates students' knowledge and skills acquired through coursework in mechanical engineering, emphasizing the design and manufacturing of mechanical components using CAD software. The challenge seeks to establish itself as a benchmark certification in the field of mechanical CAD design, particularly within the context of electronic packaging and electro-mechanical systems.

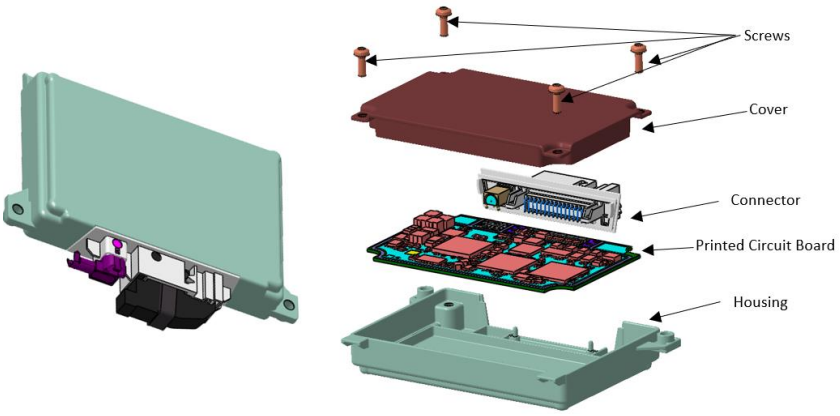


Figure 1. Electro-mechanical assembly

Objectives:

- Stimulating student's interest in mechanical engineering and CAD design, particularly in the context of electronic packaging and electro-mechanical assembly.
- Evaluating student's CAD design skills within a competitive framework, fostering a spirit of excellence and innovation in mechanical component design for electronic systems.
- Certifying student's CAD proficiency endorsed by industry experts, including the Industrial -Advisory Committee (IAC), to meet industry standards and requirements for electronic packaging and electro-mechanical assembly.
- Providing the electronics industry with a pool of skilled CAD designers ready to contribute to various electro-mechanical engineering projects, including electronic packaging solutions.
- Familiarizing students with the processes involved in designing mechanical components and assemblies for electronic packaging, ensuring compatibility with electronic modules and adherence to packaging standards.
- Cultivating a high level of professionalism in the use of CAD software systems for mechanical engineering applications in the context of electronic packaging and electro-mechanical assembly.

- Increasing awareness within the mechanical engineering and electronics industries about available talent and fostering strong partnerships between academia and industry in the realm of electro-mechanical engineering.
- Generating increased demand for mechanical engineers with CAD design skills specialized in electronic packaging and electro-mechanical assembly among current students and expanding job opportunities within the industrial sector.

Description of a subject (summary)

As a mechanical design engineer, your company won a project to create a sensor module for a well know OEM car manufacturer. To boost profits and speed up development, the company chose to use existing components (Figure 2) and make design ajustments to meet the client's needs. Modifications to the bracket and sensor ensure they fit within specified areas without altering overall functionality. The client provided a 2D drawing ("Cover.pdf") as a starting point for the cover design, which must be optimized to meet all requirements. The 3D model includes restricted areas for the new parts.

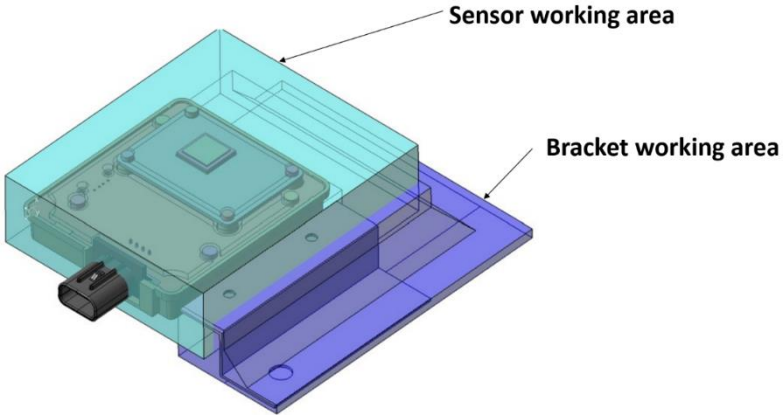
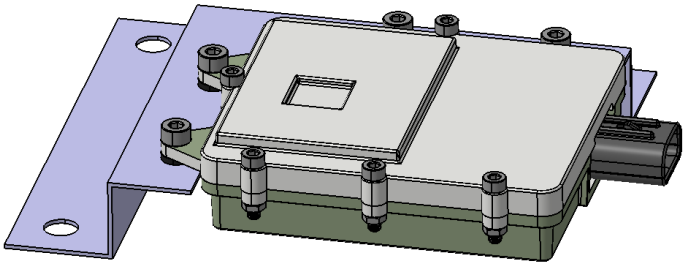


Figure 2 Existing components

Solution



The criteria on the basis of which the student qualifies as being initiated in the evaluated topic:

- Understanding Electronic Packaging: Show knowledge of how to place electronic components and manage heat within CAD designs.
- Efficient Component Integration: Ability to seamlessly integrate electronic parts into mechanical designs while meeting industry standards.

- CAD Proficiency: Expertise in using CAD software to design, model, and simulate electronic assemblies.
- Creative Problem-Solving: Demonstrate innovative solutions to electronic packaging challenges within CAD designs.
- Detail-Oriented Design: Attention to detail in CAD designs, including precision in measurements, accurate placement of components, and consideration of assembly constraints and tolerances for electronic packaging.
- Compliance with Standards: Ensure that CAD designs meet industry standards and client requirements.
- Clear Communication: Clearly convey design intentions through CAD drawings and documentation for effective collaboration.
- Professionalism: Maintain professionalism by meeting deadlines, accepting feedback, and handling information ethically.

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2023	Teodor COPORAN	Politehnica Bucharest
2022	Dan-Andrei LUCA	Politehnica Bucharest

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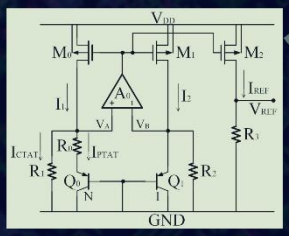
UNIVERSITATEA TEHNICĂ DIN CLUJ-NAPOCA

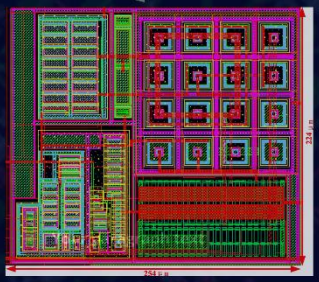
TIE n

1st edition

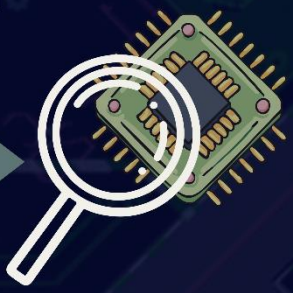
24th of April 2026
Cluj-Napoca, Romania

TIE TECHNOLOGIES of INTERCONNECTIONS in ELECTRONICS
Industry-wide Student Challenges
A WAY to turn your HOBBY into PROFESSION





DRC
LVS
PEX



AUMOVIO
Infineon
MICROCHIP

TIEn (nano)- the newcomer at the TIE Platform -international education platform for students and talents in electronic packaging-

Today, the European Union is facing a severe shortage of skilled talent required to support the EU Chips Act. The Important Project of Common European Interest (IPCEI) provides an excellent framework to enhance and foster the development of the semiconductor industry in the EU, helping to meet the growing demand for trained engineers in this field.

At the national level, the Romanian Government has undertaken initiatives to financially support these projects, aiming to transform the country into a relevant player in the microelectronics sector. Although the semiconductor value chain cannot be fully internalized, segments such as design, physical implementation (layout), testing, and circuit validation can be successfully executed within Romania.

Developing these activities requires close collaboration between engineering universities and the industrial sector to equip future engineers with up-to-date and relevant skills. **Figure 1** presents a reduced set of activities involved in the integrated circuit development process, illustrating the flow required to develop a functional module for chip integration.

For years, the Technologies of Interconnection in Electronics (TIE) platform has connected Romanian universities with the electronics industry to cultivate specialized talent. Building on this legacy, extending the competition to include **TIE-n (nano)** is a strategic step. By combining micro- and nanotechnologies, TIE provides a robust ecosystem for assessing student knowledge, ranging from integrated circuits and System-in-Package (SiP) technologies to complex PCB design. Beyond education, TIE serves as an industry-recognized challenge, certifying that students possess the electrical, mechanical, and thermal design skills demanded by the market.

Within the framework of the **TIEn** challenge, the process begins with Schematic Capture based on established standards, using PDK components and documenting critical layout constraints such as electromigration requirements, device matching, and noise sensitive nodes. Once validated, the schematic is transitioned to the layout phase, where the designer implements decisions regarding device matching (e.g., common centroid), optimal routing (including shielding and star connections), and floor planning. Following the initial layout iteration, the design undergoes three standard Physical Verification steps, i) DRC (Design Rule Check), ii) LVS (Layout vs. Schematic), and iii) PEX (Parasitic Extraction), which are essential for evaluating the implementation quality. Once the

physical design passes all checks and meets the required specifications, it is integrated into the full chip for final verification and GDSII file generation for fabrication.

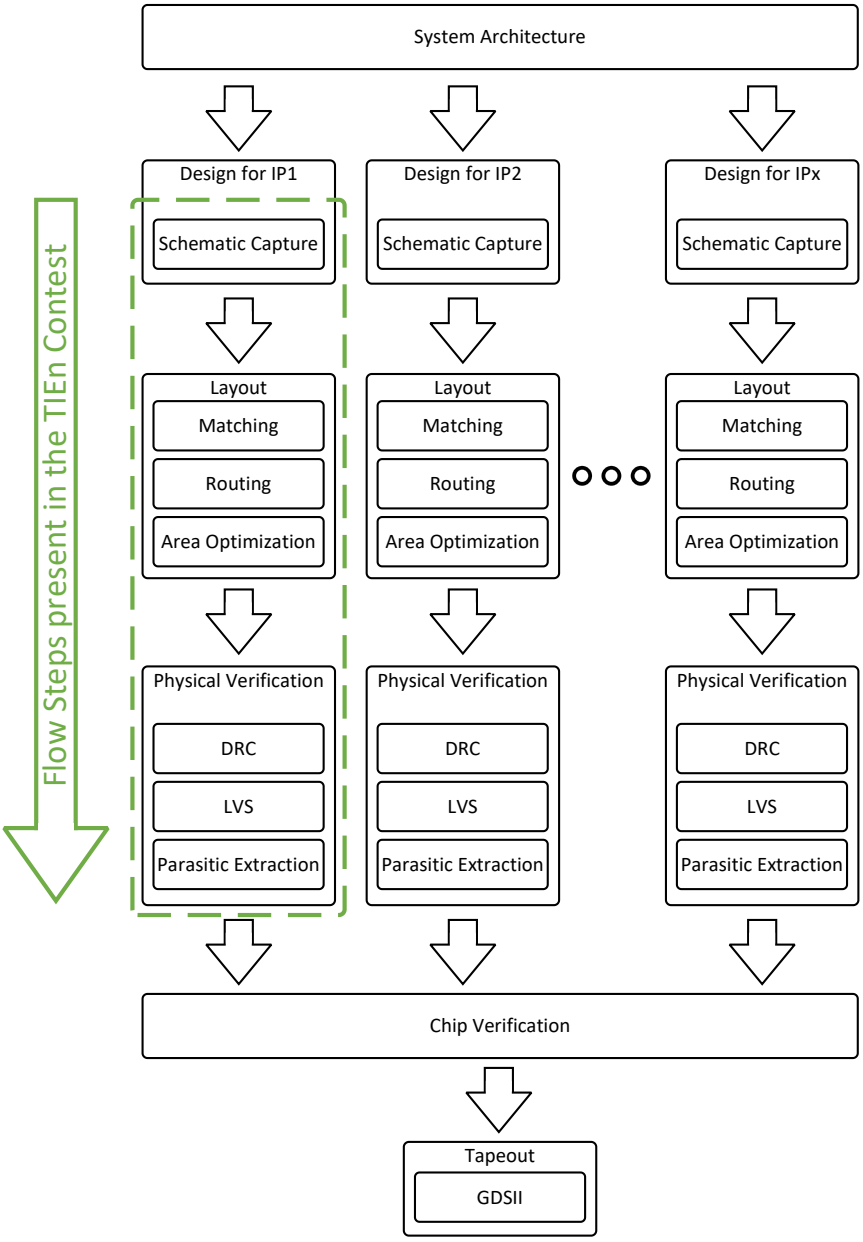


Figure 1 – Integrated circuit development flow

The transition to deep-submicron technological nodes introduces major complexities in the physical implementation stage. Design efforts face obstacles generated by manufacturing process limitations (such as WPE, STI stress, and matching issues), the

influence of parasitic elements (RC), and thermal constraints caused by increased power density. Since these phenomena directly degrade circuit performance, the responsibility for mitigating them falls predominantly on the physical design and layout implementation stage.

This rigor in physical implementation becomes even more critical in the era of chiplet technologies, a strategic direction supported by the Romanian Government through funding instruments such as IPCEI ME/CT and POCIDIF. Layout activity for IP blocks forms the foundation for generating chips that are subsequently integrated into these advanced heterogeneous systems, which are essential for artificial intelligence and data processing. Thus, physical design competencies contribute directly to consolidating a competitive national ecosystem that unites universities, research centers, and industrial partners.

Starting in 2026, the TIE family of contests takes a significant step toward cultivating integrated circuit development skills by launching the TIEn (nano) section. This section is dedicated to physical design (layout) for analog and mixed-signal circuits. The objective will be achieved by organizing a national student competition that involves implementing an analog module according to industry standards. The results will be validated by a committee composed of experts from both the private sector and academia, possessing extensive experience in the field. Thus, closing the gap between two major contributors for developing reliable electronic products, the IC designers and the product engineers.

Cosmin MOISA,
Design Center Manager,
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TIE$_n$ - Committee

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Mircea STOICA, Microchip Technology București
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National University of Science and Technology
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www.upb.ro

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Invented for life

Gh. Asachi Technical University of Iaşi

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www.2dphotonics.com

Graphene integrated photonics — Revolutionising Generative AI with energy-saving optical interconnects for smarter scaling and a sustainable future.

2D Photonics designs and manufactures graphene-integrated photonic integrated circuits and complete optical systems for datacentres and telecoms. Our foundry-compatible solutions enable compact, energy-efficient optical transceivers and interconnects that scale bandwidth for Generative AI and HPC while lowering power and cost per bit.

The problem

As AI and HPC scale, copper links hit range and energy limits; complex electronics increase cost and thermal burden. Optical interconnects are required to connect GPUs and HBM efficiently.

Our solution

Graphene Integrated Photonics (GIP) — single-crystal graphene integrated into modulators and detectors at foundry-compatible yields, enabling optical transceivers with reduced electronic complexity, higher channel density and lower energy per bit.

Breakthrough / IP

Demonstrated high-performance photonic integrated circuits (PICs) with single-crystal graphene in both detector and modulator elements — yields and performance suited for commercial transceivers.

Traction & partners

Corporate investors and partners include Sony, CDP, NIF, Frontier IP, Indaco, Join Capital and others.

Key technical advantages

- High bandwidth density — ultra-fast electro-optical response for compact, dense channels.
- Wavelength-independent design — single design across O, C and L bands.
- Low power consumption — uncooled operation and low insertion loss.
- High traffic capacity — broad wavelength operation for WDM scaling.
- Foundry compatible — processes align with silicon photonics foundry tooling.

Applications

- Generative AI datacentres: low-power optical links between GPUs and HBM.
- Telecom & datacom transceivers: higher density, lower latency optical modules.
- Mobile and edge data transfer where efficiency and resiliency matter.

Visit 2D Photonics — www.2dphotonics.com

AUMOVIO is a new brand and an adaptive force shaping the future of safe, exciting, connected, and autonomous mobility. Built on 150 years of technological and mobility innovation, the brand is further strengthened by over 25 years of proven experience in Romania.

As of September 2025, AUMOVIO operates as an independent company, continuing the legacy and expertise of the former Automotive sector of the Continental Group. Active in the automotive industry, AUMOVIO has a strong presence in Romania, with four research and development centers located in Brașov, Iași, Sibiu, and Timișoara, as well as two production facilities in Sibiu and Timișoara.

The AUMOVIO team in Romania numbers approximately 12,000 employees, more than half of whom are engineers and IT specialists contributing to innovation within the R&D centers.

AUMOVIO Sibiu plays a key role in this ecosystem, serving as a strategic hub for innovation and a trusted global partner for the automotive industry. The location manufactures around 40 million electronic control units annually, while also developing, testing, and producing advanced solutions such as intelligent braking systems, driver assistance technologies, and connectivity systems.

In Sibiu, complex projects take shape across the entire technology spectrum—from software and hardware development, testing, process and mechanical engineering, and simulation, to cutting-edge fields such as cloud technologies, artificial intelligence, and cybersecurity.

Discover AUMOVIO Sibiu: https://www.youtube.com/watch?v=7vAhGOxV4Cs

Technique for a lifetime

BOSCH

Bosch Engineering Center in Cluj

Since its establishment in 2013, the Bosch Engineering Center in Cluj has played a key role in the great transformation of the mobility sector. With its extensive expertise in software, hardware & mechanical engineering and reliability engineering, as well as in sales planning, the center contributes to the development of innovative products and services based on artificial intelligence (AI) applied in the fields of automated driving, electric and connected mobility.

Whether it is advanced driver assistance systems, electric power steering systems, traditional and electric propulsion systems, various services for the automotive industry - we have extensive experience in developing innovative software and hardware solutions. We are also a leading leader in the field of artificial intelligence technology in the automotive industry with the largest team of AI specialists in Romania.

Thanks to complex technical projects, our contribution to the development of innovative Bosch products, professional and personal development opportunities for colleagues, flexible working methods, modern offices and laboratories in Cluj-Napoca and Jucu, we are one of the most sought-after employers among engineers and IT specialists in Romania.

Our promise to our colleagues is a firm one: we develop together, enjoy our work and inspire each other.

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ICCO EMT, is a leading technical distributor of equipment and related materials to the microelectronic & advanced technology sectors, as well as electronic assembly having solution from Kulicke & Soffa, OMRON, AMX and Nano Dimension.

Our commitment is to provide our customers with first-class technology and complete services, from the configuration and the supply of the equipment, continuing with installation, programming, and maintaining the equipment, and finally, concluding with training the customer's personnel and supporting the customers during the product ramp-up period.

Due to the high diversity of the products we offer to our customers, we are now able to configure and provide turn-key solutions for electronic production, fully functional manufacturing lines, including ball bonding, wedge bonding, advanced dispensing solutions, sintering process, P&P equipment, electronic testing equipment, wave and reflow ovens, coating systems, electronic production automated machinery, soldering repair, rework tools.

We offer integrated electronic assembly services, SMT and THT technologies, complemented by testing, engineering services and box build. Our modern automated inspection equipment (SPI, AOI-3D, X-ray) and functional testing ensure high quality standards for every order. Our quality standards are certified ISO 9001:2015 and IATF 16949:2016.

ifm – Technology, Innovation and Quality in Automation

The German group **ifm**, a global leader in the development of sensors, automation systems and digital solutions, is present in Romania (Sibiu) through three divisions:

- **ifm efector** – production of position sensors
- **ifm prover** – production of process sensors
- **ifm electronic** – sales division

Founded in 1969, **ifm** combines the strength of an international group with the flexibility of a medium-sized company, with 9,005 employees in 150 countries..

What defines us?

✓ Open and people-oriented management
✓ Fast and efficient decision-making
✓ Investments in employee development
✓ Modern work environments
✓ Promoting a healthy lifestyle

Our mission is to become a benchmark in the Western Industrial Zone of Sibiu, being not just a supplier, but a trusted partner for customers and an exceptional employer.

ifm values:

✅ **Innovation** – Cutting-edge technology for automation
✅ **German quality** – Reliable, rigorously tested products
✅ **Customer orientation** – Personalized consulting
✅ **Sustainability** – Energy-efficient solutions

ifm solutions for industry:

- **Industrial sensors** – proximity, position, pressure, temperature detection
- **Diagnostic systems** – monitoring and predictive maintenance
- **Controllers & IO-Link** – efficient communication between devices
- **Software Industrie 4.0** – real-time data analysis

Industries served:

- **Automotive** – Automation and quality control
- **Food industry** – Production process safety
- **Logistics & Transport** – Smart Monitoring
- **Energy & Environment** – Efficiency and Sustainability

At **ifm**, we continuously innovate to contribute to a more efficient and sustainable future!

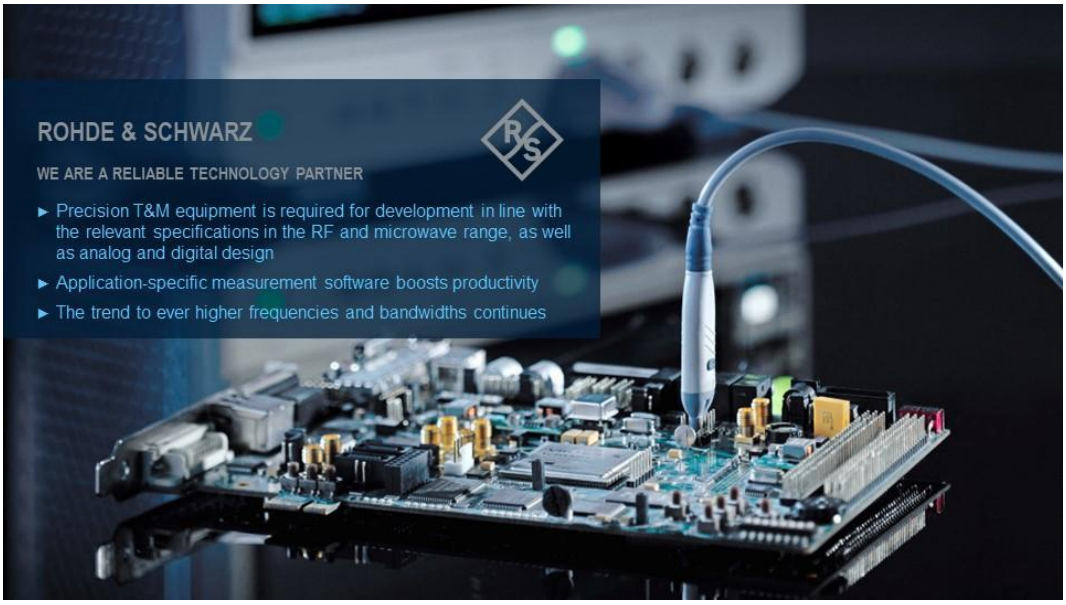
As a world leader in secure connectivity solutions for embedded applications, NXP Semiconductors is pushing boundaries in the automotive, industrial & internet of things (IoT), mobile, and communication infrastructure markets while delivering solutions that advance a more sustainable future.

The company has had substantial growth over the last few years, with currently 1100 team members at NXP Romania in Bucharest and Sibiu.

NXP Romania contributes to the development of solutions for automotive, consumer and industrial IoT markets by developing software platforms that integrate NXP components and software from partners. In addition to software development, NXP also invests in research as part of intellectual property creation programs.

Each year, NXP Romania hosts interns who learn the specifics of software development in Automotive, Edge Computing and IoT. We are proud that our interns extend their experience with practical contributions in real-life projects.

Search for latest internship openings on:



Rohde & Schwarz is a global technology group striving for a safer and connected world. With its Test & Measurement, Technology Systems and Networks & Cybersecurity Divisions, the company creates tomorrow's innovations today. The company's leading-edge products and solutions empower industrial, regulatory and military customers to attain technological and digital sovereignty.

Innovation has been part of Rohde & Schwarz since the very beginning. The company founders Dr. Lothar Rohde und Dr. Hermann Schwarz were technological pioneers. With their hands-on entrepreneurial spirit, the two college friends entered the unexplored field of RF engineering. Ninety years later, the company is still pushing technological boundaries – as a successful shaper of cutting-edge technologies such as artificial intelligence (AI), 6G, cloud and quantum technologies.

The privately owned company is known for stability and resilience. Independence is at the core of its entrepreneurial identity. The company finances its growth with its own resources. Because the company does not have to think in terms of quarterly results, it can plan sustainably for the long term. The high added value of Rohde & Schwarz makes the company a reliable, trustworthy and relevant partner for its customers.

TEST & MEASUREMENT	**TECHNOLOGY SYSTEMS**	**NETWORKS & CYBERSECURITY**
Wireless I Industry, Components & Research I Aerospace & Defense Testing I Automotive	Secure Communications I Critical Infrastructure & Networks I Government I IP Network Analytics I Broadcast, Amplifiers & Media	Endpoint Security I Secure Networks I Certified & High-Grade Crypto Solutions

Keytek Innovation is a design house capable of ensuring the development, security, and efficiency of custom electronic systems from idea to production, regardless of any challenges that may arise during the process. Our analytical skills and critical thinking, combined with a solid background in electronic engineering and hardware system design, will help you reduce time-to-market while keeping the development process cost-effective.

At Keytek, we boast extensive experience in High-Density Interconnect (HDI) PCB design, and we utilize cutting-edge 3D Electromagnetic (EM) analysis software and circuit simulation tools to perform signal and power integrity analysis. We understand the importance of this in today's digital world, where new standards require higher data rates, faster speeds, and increasingly complex designs. To shorten the debugging time, ensure product performance, and preemptively address future issues, our design process includes a comprehensive suite of analysis and verification techniques. Ensuring consistency, repeatability, and reproducibility are our primary objectives when validating and verifying various systems. To guarantee the success of these processes, we utilize measurement instruments from industry-leading companies and post-process the results using various programming languages specifically designed to streamline the validation and verification steps.

Building the Future of Data Infrastructure

Marvell Technology, Inc. (NASDAQ: MRVL) develops and delivers semiconductor solutions that move, store, process and secure the world's data. As a trusted leader in essential data infrastructure semiconductor technology, Marvell's cloud-optimized silicon powers innovation in cloud and AI, carrier infrastructure, automotive and enterprise networking markets. With a comprehensive portfolio of electro-optic, Ethernet, processor, security and storage products and IP, the company offers merchant, semi-custom and fully custom options to address a range of customer requirements.

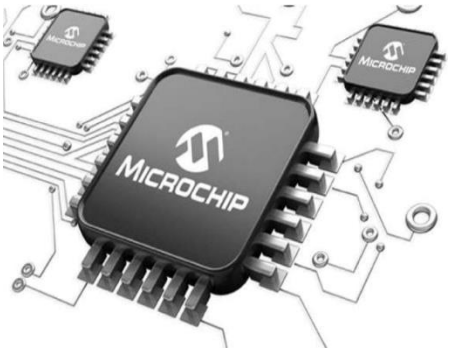
- Fabless semiconductor company
- Innovating since 1995
- 10,000+ patents worldwide
- Headquartered in Santa Clara, California
- Research and development centers located in USA, Israel, India, Vietnam, Argentina, Italy, Canada, Germany, and China
- Focused on excellence in Engineering with 85% of employees in technical roles

To learn more, please visit us at www.marvell.com.
Scan the QR code to view the Marvell 101 video.

Microchip Technology Inc.

Microchip Technology is a leading provider of smart, connected and secure embedded control solutions. As a global company with over 20,000 employees, Microchip has a robust presence in Romania. Our company has an extensive portfolio that includes advanced **microcontrollers, digital signal controllers, microprocessors, mixed-signal, analog, interface, and security solutions**. Our innovative solutions empower a diverse clientele, serving customers across key sectors such as **industrial, automotive, consumer, aerospace and defense, communications, and computing**.

Romania Design Center (RDC) – A Hub of Technological Excellence



At the heart of our innovation lies the **Romania Design Center (RDC)** a crucible of talent and expertise accommodating over **multiple business units**. Furthermore, it is a nucleus for **software development, field technical customer support**, and the design and application development of **8-, 16-, and 32-bit microcontrollers and microprocessors**.

Strategically located in the **AFI Business Park,** adjacent to the Electronics, Telecommunications and Information Technology (ETTI), the RDC is not just a workplace but a nurturing ground for budding engineers.

TRiREME
DIGITAL & GREEN SKILLS TOWARDS FUTURE OF THE MOBILITY ECOSYSTEM

Co-funded by the European Union

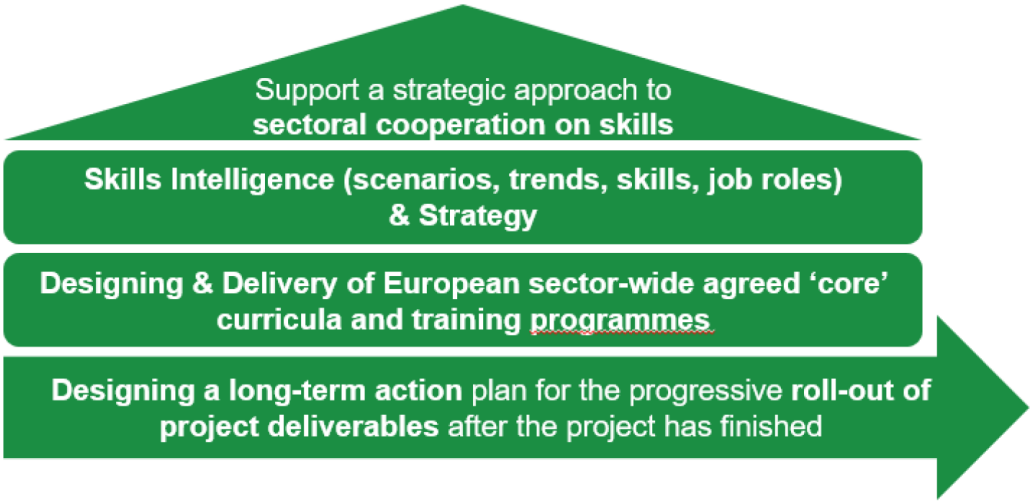
TRIREME Project

DigiTal & GReen SkIlls TowaRds FuturE of the Mobility Ecosystem

TRIREME is a 4 year Erasmus+ funded project aimed at developing tools and activities to enhace skills and foster collaboration within the automotive sector, facilitating the transition towards a greener and more digital future. The project aligns with the European Pact for Skills and its respective large-scale Partnership, the Automotive Skills Alliance.

4-year **ERASMUS+ Blueprint** Project (2024 – 2028)

31 project partners from the **Automotive Skills Alliance** partnership



Support skills agenda in the Automotive-Mobility Ecosystem through the Large-scale Pact for Skills Partnership

AUTOMOTIVE SKILLS ALLIANCE

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APTE

ELINCLUS ELectronic INnovation CLUSter

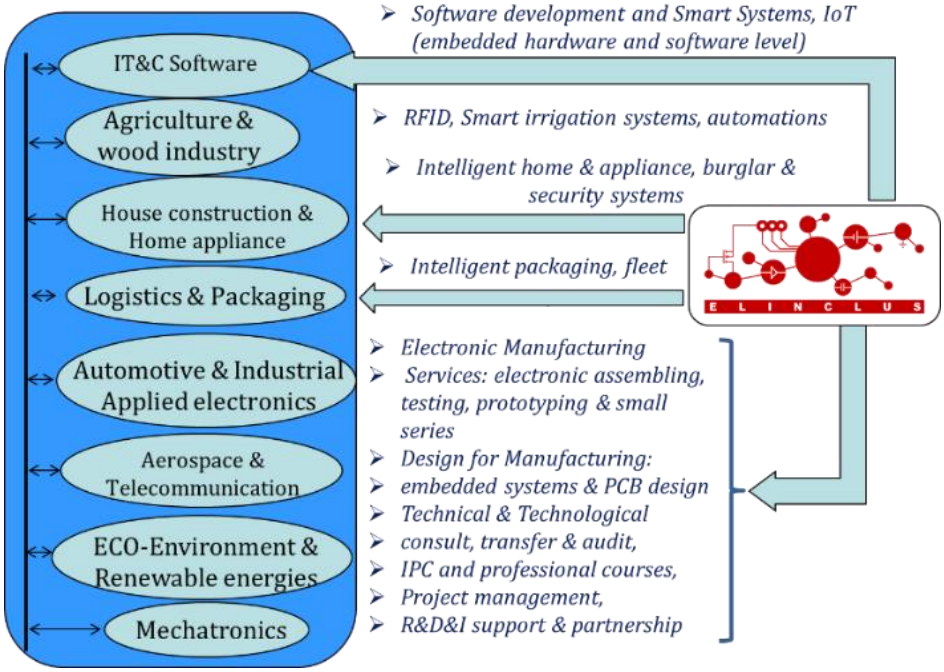
EMC: Association for Promoting Electronics Technology – APTE (www.apte.org.ro)

Founded 2011; 94 registered members

President: Prof. DHC. mult. Paul SVASTA,Ph.D.

Executive Manager: Lect. Eng. Bogdan Mihăilescu, Ph.D.

- Founding member of the Clusters Association from Romania, CLUSTERO - www.clustero.eu
- European Cluster Excellence Initiative Silver Label Certificate from ESCA since 2016
- Founding member of the IT Cluster Network from Romania comprised of 9 members 9: Transilvania IT Cluster, ALT – Brașov, Banat Software, Innovative Clsuter Open Hub, INOMAR, **ELINCLUS**, ICT Oltenia, ICT Cluster Lower Danube și Smart Alliance Cluster.
- Founding member of the regional Digital Innovation Hub – Smart e-Hub https://smartehub.eu/



- **E-mail**: office@elinclus.ro **Web page**: **www.elinclus.ro**

ASSOCIATION FOR PROMOTING ELECTRONICS TECHNOLOGY (ASOCIAȚIA PENTRU PROMOVAREA TEHNOLOGIEI ELECTRONICE)

IMAPS ROMANIA

A globally-competitive workforce with theoretical, as well as applied engineering/hands-on, education must be trained. In addition to the areas of science, engineering, microelectronics, and packaging, this training must encompass the broader areas of business, economics, ethics, foreign culture, and languages.

The Association for Promoting Electronics Technology (APTE, see https://apte.org.ro/) is IMAPS Romania. APTE was founded in 2002, by the Center for Technological Electronics and Interconnection Techniques (CETTI) together with highly respected members of the electronics industry, in order to support the electronics packaging education and engineering, in a climate of trust, ethics, and social responsibility.

APTE/IMAPS Romania is the management entity of the ELINCLUS Cluster (see http://elinclus.ro/), which has currently 94 members. ELINCLUS was established starting from the economic relationship existing between CETTI (which developed a Technological and Business Incubator, entity accredited by the National Innovation and Technology Transfer Network – ReNITT) and companies from Bucharest and Ilfov county. This structure has offered to ELINCLUS the status of a regional cluster in the field of electronics.

APTE offers annually a comprehensive set of short courses and training classes in the area of electronics packaging, IPC standards certification, management, and industrial development, in order to serve the needs of the electronics industry. APTE organises annually The International Symposium for Design and Technology in Electronics Packaging (SIITME, see http://siitme.ro/) and the Technologies of Interconnection in Electronics (TIE, see www.tie.ro/) Industry-Wide student challenges.

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ITEC Information Technology in Electronics Research Center

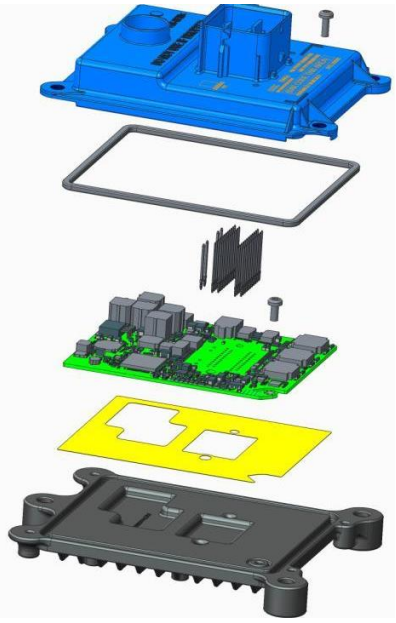
TECHNICAL UNIVERSITY OF CLUJ-NAPOCA ROMANIA

ITEC Research Center

belongs to the Technical University of Cluj-Napoca having 25 researchers in Embedded Systems (electronics & software). ITEC can access the entire infrastructure of Technical University of Cluj-Napoca, resources from all other research centers and resources from Romanian University Alliance.

ITEC Competencies

- Circuit design: modeling, simulation and cross-simulation of electronic circuits (analog, digital, power, RF/EMI) & system design: modeling and simulation for electro-mechanical systems: power devices, actuators, mechatronics;
- HW Application design: fast-prototype design, PCB design for mass production, BOM/AVL design, DfM & DfT for embedded applications, power supplies, interface/signal conditioning boards;
- SW Application design: embedded control applications for OS and non-OS targets;
- TW Application design: testing and design of testing systems: SW and HW testing process, HiL and SiL, design of test-cases for SW;
- Training services: LabVIEW trainings, Embedded Systems trainings, TW and HiL operation;
- PCB DESIGN: DfX, SI and PI.



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Welcome TIE 2027 – Ștefan cel Mare University of Suceava!

Since its first edition, the TIE contest has fulfilled its original goal, forming a powerful bridge between academia and the industrial sector. Participants gain a solid start in electronic design through schematic and layout, signal analysis, power distribution, and more, forming a strong foundation for a successful professional career.

The recent competition topics are complex and comprehensive, posing a true challenge for students, as they require advanced knowledge of electronic packaging. When involving industry members, these topics become tangible, demonstrating real-world applications of electronic devices. This approach offers students new insights beyond just using CAD software, allowing them to see the actual, finished product from the competition task. Participating in this event can be a valuable experience for students eager to expand their understanding and prepare for industry challenges.

In conclusion, whether I speak as a current coach or a former contestant, I can affirm that TIE is more than a method—it's a lifestyle that brings together students, trainers, and experts in electronic packaging.

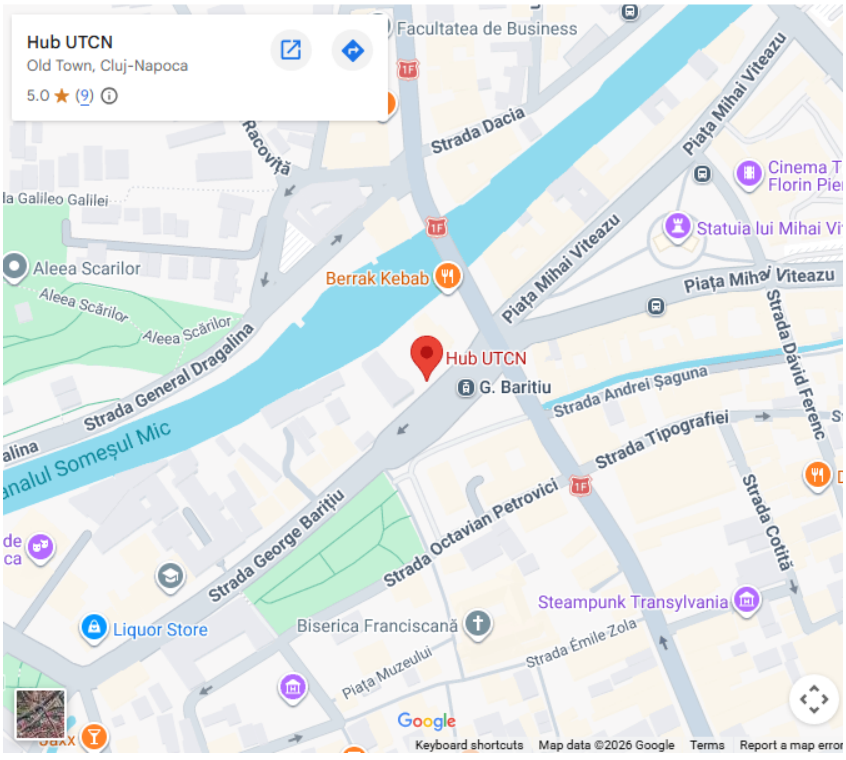
We look forward to welcoming you to Suceava for TIE 2027 and to enjoying the unique charm of this historical city!

April 17th, 2026

Local Organizing Chair:
Assist. Prof, **Adrian-Ioan PETRARIU**, PhD,
Ştefan cel Mare University of Suceava

Venue of the TIE 2026

Events Location:
HUB UTCN, George Barițiu Street 4, Cluj Napoca

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